

Multi-Project Wafer (MPW) Service Center Circuits Multi-Projets®

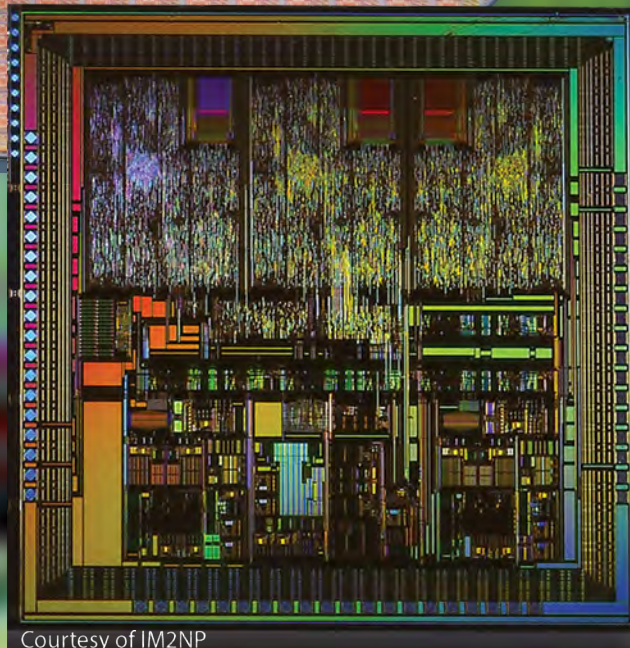
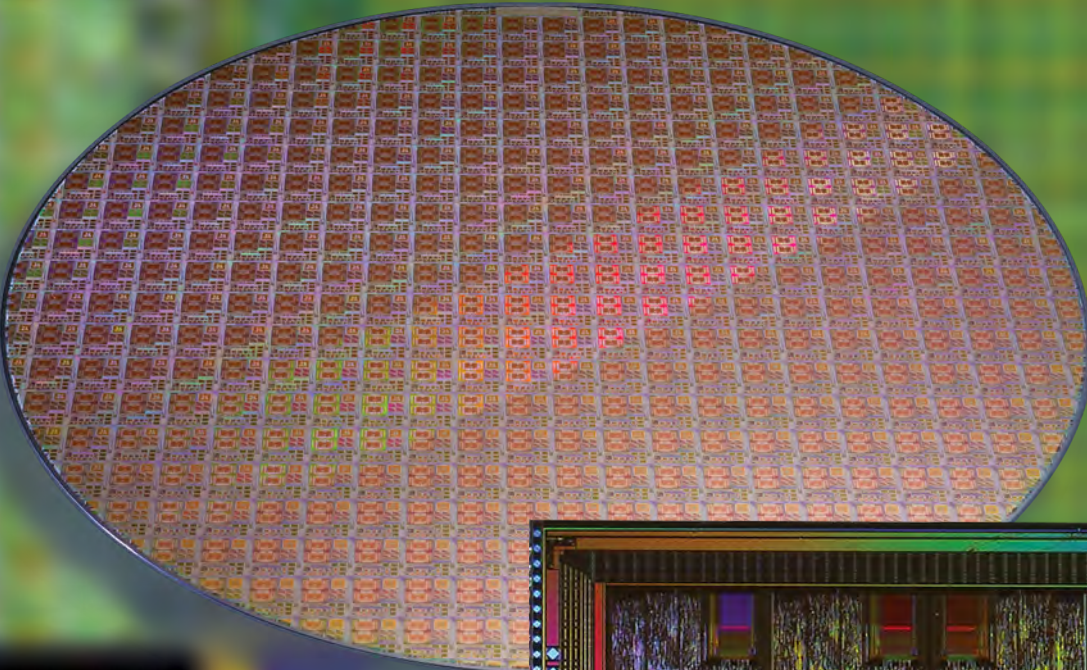


From layout to chips

Annual report 2019



<https://mycmp.fr>



Courtesy of IM2NP

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Editorial

Dear CMP users and partners,

2019 has ended after an incredible sequence for CMP for many reasons. It has also been the case for our users' community that has experienced several changes over that year. Regarding statistics, CMP reports a small increase in the number of projects. For 2019 the activity of CMP remains strong, with numerous large projects and volume productions. All in all the activity of CMP is more or less stable over the past years. Let me now focus this Edito on some important topics regarding 2019.

First of all, because it is important to highlight and because I believe this is really an important move, and evolution, for CMP and its community, there is now one year that we are part of the Europractice (EP) program and proud of it. Please, do not believe that it is simple and straight forward, but it is and it will become a success story for us, for Europractice, and of course, for you and for the community. We have spent a lot of time together with the other EP partners, to align our workflows, practice and strategies. We are not completely there, but we are on our way. CMP providers are now visible on Europractice web site, for their benefits. Our users get discounts and better supports thanks to the European community. We are advertising together with the other EP partners, we are building the best CAD and technology portfolio Europe could imagine and wish. More is coming and I hope we will reach Users, Providers and Funders expectations!

Over 2019, CMP has operated its service through our new web application myCMP. I know that not everything was operational from the first use, but at the same time, this is a real move forward that we have initiated. By the time I'm writing this Edito, 249 CMP service Users, meaning Institutions, are registered in the web-app. We have managed almost all our 2019 MPW runs through myCMP. We are about to integrate all the administrative and financial toolboxes together with the support center/hot line in the application, leading to a unique and unified interface between CMP employees, operating the services, and CMP Users. We are still not fully stable with this new tool and its implementation and usage but this will definitively bring quality services in a near future.

2019 has also been an important year in terms of new services and technology partnership prospection. By the time this editorial is written, it is not less than four new partners and/or new technologies that are now available through CMP. And more is coming in a near future. We are actively in contact with microelectronics ecosystem leading players as well as niche technology actors trying to aggregate a complete and complementary portfolio, to answer our Users' community needs. The dynamics that was growing internally, amplified by Europractice partnership has produced positive results. Also, this year we have initiated an important "support program" with our partner STMicroelectronics in the frame of IPCEI-Nano2022, in order to sustain and to develop the MPW services on advanced technologies. Still not quite totally visible in 2019, this will be felt in the coming years with a more reliable MPW run schedule, better follow-up on schedule and more on supports.

I cannot end this editorial without mentioning that it is my last contribution, as CMP Director to the CMP annual reports. I leave CMP by the end of 2019, after seven years, trying my best to keep CMP in the heart of the national, European and worldwide R&D microelectronics community. I have been working with the team, with providers and suppliers, partners and others, to make it happens. I leave with a great professional experience, I have learnt a lot and I really hope, that you, who are reading these lines, are satisfied about the job I/we did. My colleague, Kholdoun Torki, with whom I have managed CMP over the past years, is going to take the responsibility after me. I wish him, and the whole CMP team, the best for the coming years. And I also wish CMP Users, nice piece of works through CMP services.

Jean-Christophe Crébier

Circuits Multi-
Projets® (CMP)
Multi-Project
Circuits®

From Layout to Chips

mycmp.fr

Overview

A large number of complex manufacturing steps are required for Integrated Circuits fabrication, but mass manufacturing them on a wafer make these circuits cheap. Since most of the technological steps are repetitive and are carried out for a very large amount of components. Each processed wafer of silicon is cut into hundreds of dices. For some of the slowest and costliest operations, “boats” of hundreds of wafers are processed together. This means that tens of thousands of circuits are fabricated simultaneously. With such a high number, chip fabrication units cannot tolerate relatively low yields.

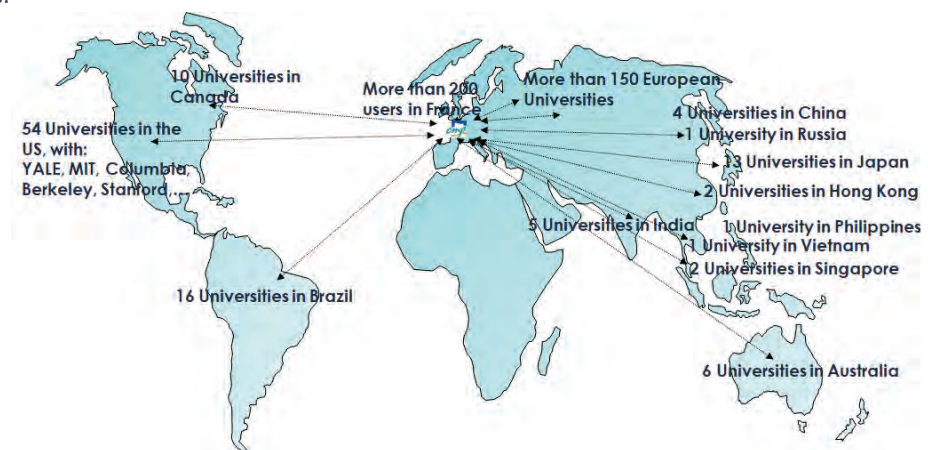
For non-collective operations, such as prototyping, test and packaging, the chip mass production techniques are highly automated and costly. These very expensive techniques seem out of reach for research and educational centers for low volume integrated circuit prototyping. Hence it is necessary to come up with an economically viable solution by means of which research institutions can get their circuits fabricated a research or education prototyping will only require a few chips and mass production is not necessary. In a similar manner, start-ups and companies requiring a low volume production would also be interested by such a low volume chip manufacturing proposition.

The basic idea of a Multi-Project Wafer (MPW) is to collectively process circuits that are different and dissimilar from the design point of view but share the same manufacturing technology. High fabrication costs of a wafer or wafers can then be shared. To do so, a large number of elementary circuits are placed side by side, to be reproduced on the wafer.

The fabrication yield must be excellent and at least constant since circuits cannot be tested before being sent back to the designers. A high yield is obtained through industrial production processes. Using such industrial processes, CMP was able open the MPW service to industry as early as in the year 1990, for prototyping as well as for low volume production.

Low volume production is aimed at helping Small and Medium size Enterprises - SMEs - to get relatively small number of circuits (say a few hundred or a few thousand), that they would not obtain directly from manufacturers. A MPW service center like CMP acts as an interface between the IC manufacturers and the SMEs to facilitate SME's access to advanced technologies, even the most expensive ones.

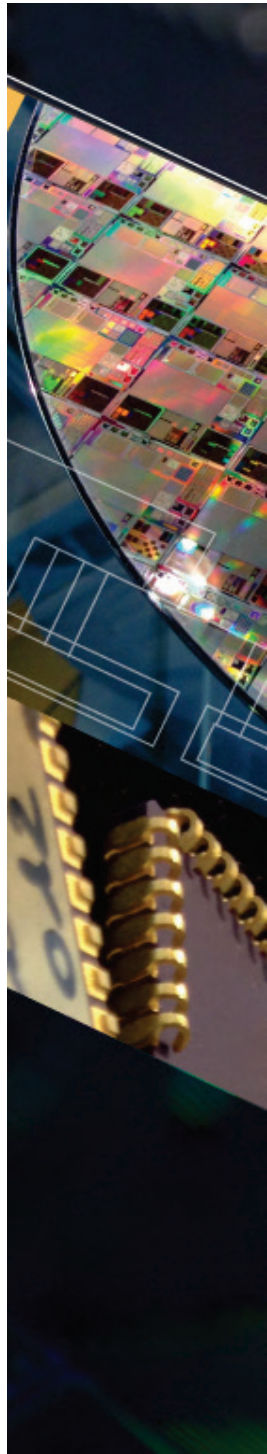
Finally two essential criteria driving CMP MPW offers must to be underlined: circuits are mostly manufactured through industrial lines and very mature and/or advanced processes. Some very innovative technologies or services are offered through recognized technological institutions with the objective to make them available to the community at an early maturity stage. From layout to delivery of chips, CMP supports a worldwide community of users to get access to such provider services.



Overview of CMP User's community around the world

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Operations performed for all projects to get access to a Design Kit (DK)

Selection of processes

Processes made available have to be selected by anticipating the demand of research institutions and for industrial prototyping.

Furthermore, maintaining a portfolio of advanced technologies requires a continual adaptation. New advanced and/or niche/specialized technologies are regularly introduced every year. Meanwhile, mature and cost attractive technologies are also of interest for R&D purposes.

After the selection of a new process all the procedures, interfaces and access conditions have to be examined, in particular:

- Which design rules could be used, and distributed
- Which standard cells are available, for what cad tools; in some cases CMP will adapt a cell library to an existing cad tool
- Which electrical measurements (pcm) will be done by the manufacturer and make available to the users,
- How circuits could be merged, scribed and packaged

Which regulations apply for this technology to send off the chip

Finally a contract is signed between CMP and the manufacturer.

Distribution and support of the design kits and design rules

Most of the design kits are delivered by CMP free of charge with the requirement that the designed circuits are to be fabricated through CMP runs.

To receive a design kit, the user fills in the appropriate form on the Web site. After acceptance, he signs the specific confidentiality agreements according to his request, and receives the design kit (normally within one or two months, depending on delays for export regulations and authorization from manufacturers). Communication of requests, legal documents and design kits are done through the internet as much as possible.

Application of the procedure flow chart

CMP complies with Procedure Flow Charts defined with provider partners, and specifically, it shall ensure, before sending any Design Kit to a Customer, that:

- A valid Design Kit Licence Agreement (DKLA) is in place between Manufacturers and CMP for the appropriate Customer, and the appropriate Technology
- A valid Confidentiality and License Agreement (CLA) is in place between the Customer and CMP for the appropriate Technology
- The audit passed regarding the VLAN security at the Customer side
- Obtaining the Export License from the appropriate administration when applicable.

CMP handles various versions and types of design kits, corresponding to the different technologies for different CAD tools. Almost all of them are free of charge.

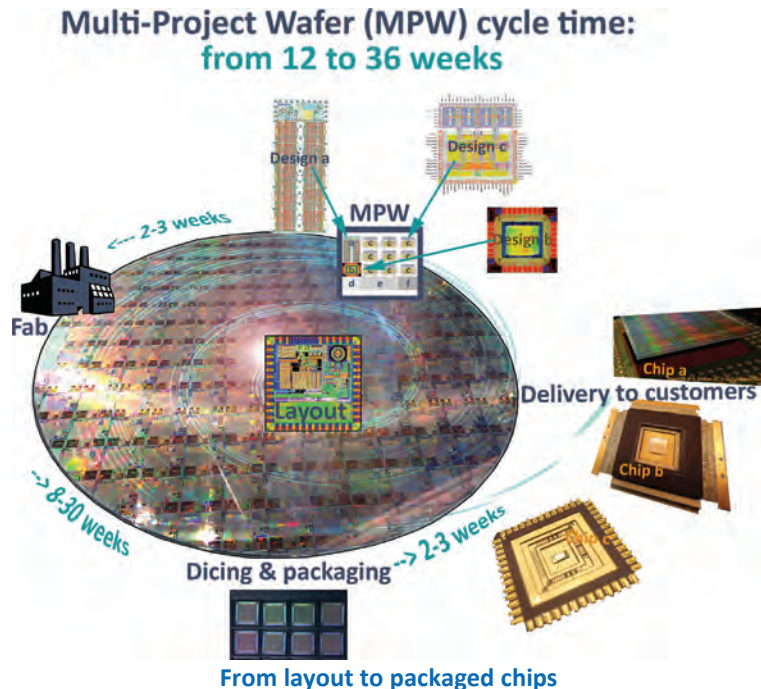
The full procedure takes at least 3 weeks and up to 2 months. For more information on the procedure to be granted access to a confidential design kit, please consult our web site: <https://mycmp.fr>

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Operations performed for all projects

To submit a design for prototyping, users are required to follow a specific procedure, intended to guaranty the compliance with manufacturing constraints.



CMP Circuit Submission Process

The procedure for circuit submission towards MPW runs has changed since February 2019. New circuit submissions will be accepted only through "myCMP" web application (<https://crm.mycmp.fr/login>). Follow the five steps described below:

1. Creation of myCMP account as soon as possible

myCMP simplifies access to all CMP services by unifying and interconnecting the various stages of MPW runs. It serves as a secure stand-alone platform for communication and documents exchange along with an automated project status tracking.

To initiate the circuit submission process, every institution must register and set up a myCMP account. It is strongly recommended not to wait until the MPW run deadline date to register and/or update settings of the myCMP designer account. This will save valuable time and avoid unnecessary stress for MPW submission. Registration to myCMP should be done as soon as a circuit tape-out through CMP is planned. Registration has to be done obviously .only once

2. Legal documents update and/or Design Kit request (FOUR WEEKS prior to the commencement of the MPW run)

All institutions are asked to pass through the Design kit request process flow in myCMP. The NDA related flow on the myCMP platform will be expedited for institutions with active NDAs in place after registration and verification. Users are authorized to submit a circuit only if a valid NDA/CLA is signed by their institution.

3. Make a reservation and place an order

3.1 Reservation request

Designers with NDAs in place willing to submit a circuit to an opened run should submit the corresponding reservation request.

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CMP staff member in charge of the run will verify and validate your reservation:

- For ST 28FDSOI and BiCMOS55 processes: Jean-François PAILLOTIN
- For ST 130nm and 65nm processes: Romain VERLY
- For ST 0.16µm process: Lyubomir KERACHEV
- For ams/em processes : Lyubomir KERACHEV
- For MEMSCAP MEMS processes: Nicolas PARTENZA
- For IRT Nanoelec/LETI-CEA / amf Si-Photonic processes: François BERTHOLLET
- For ON Semiconductor processes: François BERTHOLLET

his reservation allows run managers to organize and anticipate the required silicon area. Reservations can be canceled out any time before the MPW run deadline.

3.2. Order submission (When the design is ready)

Once the reservation is approved, an order for the circuit to fabricate has to be submitted through the myCMP account. Once this order is approved, access to myCMP FTP server will be granted through a specific account for design(s) uploading. Login credentials will be displayed on the circuit page of the active run. If packaging is required, designers should also use this interface to send their bonding diagram.

4. Design submission

The design submission can be done two weeks before the deadline, and at latest, by the deadline date. Submitted designs must be DRC and antenna error-free.

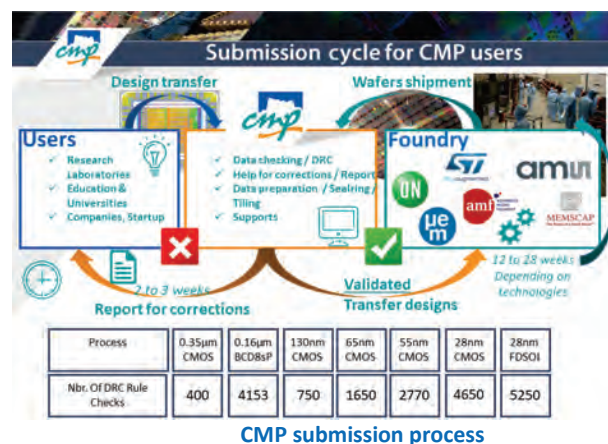
Two files are required for design submission: the design layout in GDSII format, compressed with the command "gzip -9", named "Topcell_name.gds.gz" and the "stream-out" report file generated by the CAD software during the GDSII export to be named "Topcell_name.log". We remind that these files have to be transferred via the active ftp account.

Additional information related to design transfer methodology

- Design transfer by email is not allowed without authorization from CMP.staff to ask for an e-mail transfer authorization, a request by e-mail providing designer full details and file sizes has to be submitted. CMP staff will then send instructions on how to proceed.
- Tracking the design checking process myCMP will provide the user with an overview of the design submission at every stage of the design preparation. Updates related to the submitted circuit will be provided either by e-mail or by notification on the myCMP account of the user

5. Interaction with CMP MPW manager to get design ready

Getting a design ready for post processing may require several iterations between the designer and the CMP staff in charge of the concerned run. In this case, successive design file submissions have to be done, as the first one, via the FTP server. CMP staff will then make available DRC reports through the "DRC" thumbnail of myCMP interface but may also provide via the FTP server, some other design-related files such as waivers.



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Overview of the activities in 2019

A total of 191 projects were fabricated and delivered for 82 Institutions, Research Laboratories and Companies from 22 countries.

The table below presents the turnaround times experienced through CMP on the most active technologies, based on data issued from end 2018 and 2019 MPW. These turnaround times include the time period, required after the MPW service closing date, for the data preparation between CMP and the customers and then between CMP and the manufacturer of the integrated circuits. It also includes the time for dicing and delivery worldwide of each project, without taking into account the packaging services and special requests for export licenses. For regular ceramic packaging services, please add 2 to 3 weeks lead time depending on package type and IC pads' pitch.

ams		STMicroelectronics	
0.35µm CMOS	20 weeks	130nm CMOS	20-23 weeks
0.35µm CMOS-Opto	20 weeks	65nm CMOS	28-30 weeks
0.35µm HV CMOS	23 weeks	55nm BiCMOS	28-36 weeks
0.35µm SiGe BiCMOS	20 weeks	28nm FDSOI	25-30 weeks
Including 1 to 2 weeks for data preparation and 1 to 2 weeks for wafer dicing, and prototype delivery		Including 2 to 3 weeks for data preparation and 2 to 3 weeks for wafer dicing, and prototype delivery	
MEMSCAP			
PiezoMUMPS	15 weeks		
SOIMUMPS	15 weeks		

Manufacturing times have been significantly shortened in 2019 for the ams technologies. Regarding STMicroelectronics, the delays remained stable, an effort was made on the technology 28nm FDSOI.

Hereafter are the technologies that were operated through CMP in 2019:

ams	STMicroelectronics	IRT Nanoelec/LETI-CEA
0.35µm CMOS C35B4C3	28nm CMOS028 FDSOI 8ML	Si310-PHMP2M
0.35µm CMOS-Opto C35B4O1	55nm BiCMOS SiGe 8ML	MEMSCAP
0.35µm SiGe BiCMOS S35D4M5	65nm CMOS065 CMOS 7ML	PiezoMUMPS
0.35µm CMOS High Voltage	130nm BiCMOS9MW SiGe BiCMOS	SOIMUMPS
0.35µm SiGe BiCMOS S35D4M5		

Cooperation with other services

Cooperative agreements

Over the years, CMP has signed cooperative agreement with the following National Organizations:

- CMC – Canada
- MOSIS – USA
- VDEC – Japan
- CIC – Taiwan
- IDEC – Korea

CMP distributor

- SiliConsortium Ltd. – Japan

Partnership

- MEDs – China

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Integrated circuits manufacturing

Main data in 2019

Main data concerning the circuits fabricated in 2019 are the following:

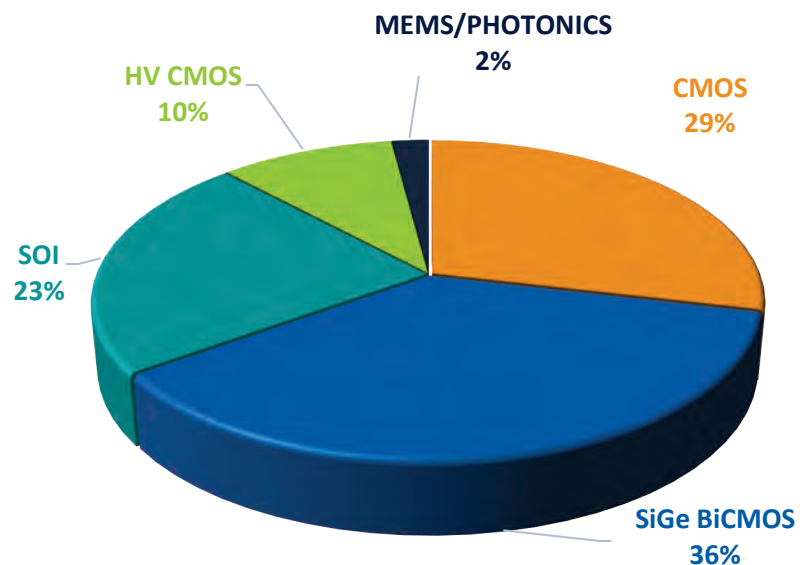
- 191 circuits for Research & Education (120) and Industry (71)
- 15 technologies in CMOS, BiCMOS, SiGe BiCMOS, SOI, CMOS and SOI High Voltage, Photonics and MEMS
- 82 participating Institutions from 22 countries
- 71 circuits fabricated for industrial purposes for 23 industrial companies
- 32 low volume production projects for 18 Institutions from fifty pieces to thousands of pieces or few wafers.

The circuit list and the list of Institutions participants (Appendix 1) are available on the web site.

Analysis of the participation

Distribution of circuits per technology and evolution

For 2019, the distribution of pure CMOS (bulk or on SOI, including High Voltage) IC projects, MEMS and Silicon Photonics IC projects is displayed below. For the second year in a row, the projects manufactured in SiGe BiCMOS technology have increased significantly to represent the largest type of circuits prototyped through CMP with 36%. This is mainly due to the greater number of projects submitted in BiCMOS055 and 130nm SiGe BiCMOS9MW, compared to CMOS (bulk or on SOI, including High Voltage) IC projects which still represents, all in all, 64% of the total.

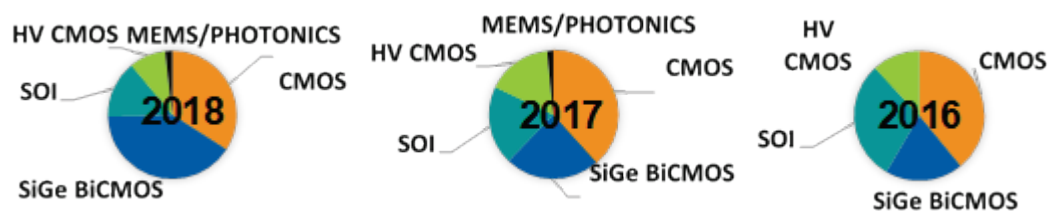


Distribution of circuits per technology in 2019

Due to a special program named NANO2022 which intend to promote 28nm FDSOI (see details in our focus), in 2019 SOI technologies represent a significant activity in volume, mostly related to the two MPW departures in 28nm FDSOI in 2019.

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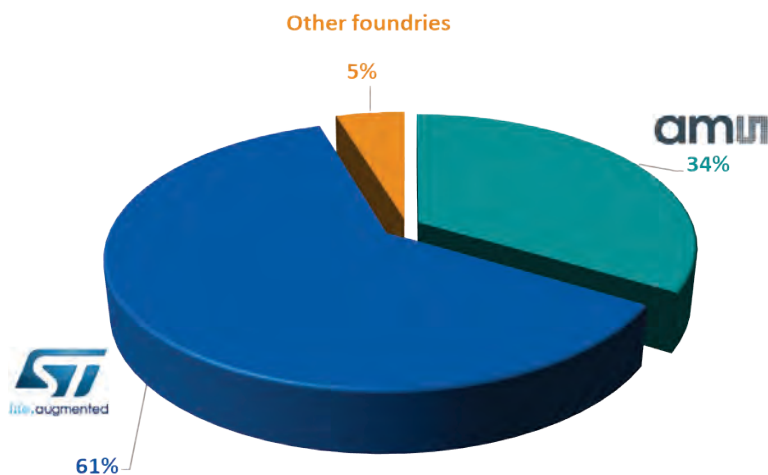


Evolution of integrated circuits distribution with respect to technology since 2016

Activity in CMOS continues to slightly decrease year after year, while activity of HV CMOS remains stable. MEMS and photonics prototypes remains marginal in volume in comparison to other technologies. The activity is stable over the year, slowly ramping up.

The number of integrated circuits submitted in regular MPW runs is higher than in 2018. A stable number of requests for re-manufacture circuits already manufactured by CMP was noted. More information about these circuits can be found in the gallery pages & CMP web site.

STMicroelectronics remains the main technology provider in our user community with above 60% of the total number of projects. STMicroelectronics IC prototyping technologies 28DFSOI and 130 nm SiGe BiCMOS9MW remain the most popular one through CMP. ams covers the remaining part with about 34%, principally with circuits in 0.35µm CMOS and SiGe BiCMOS, demonstrating how popular these mature technologies remain.



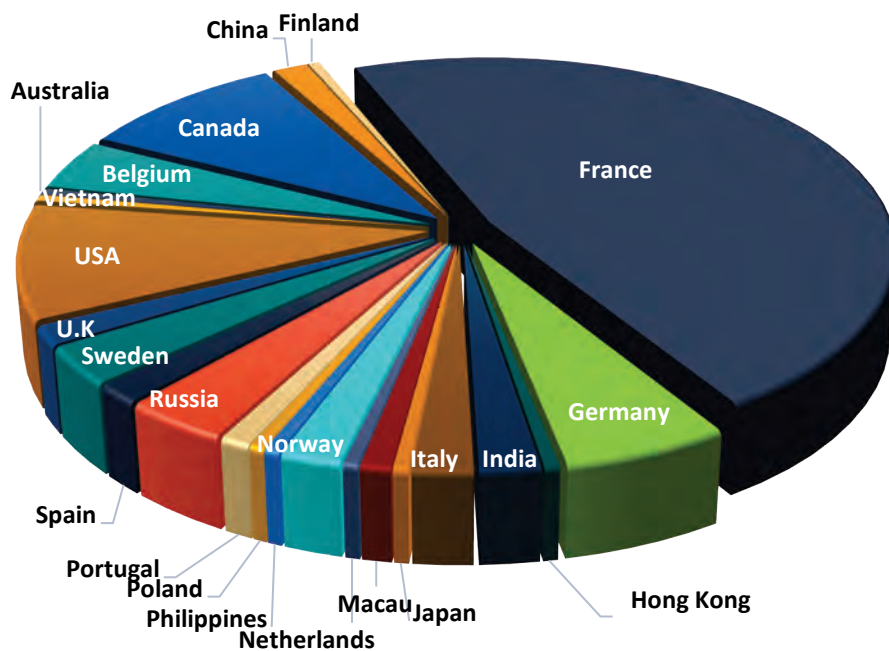
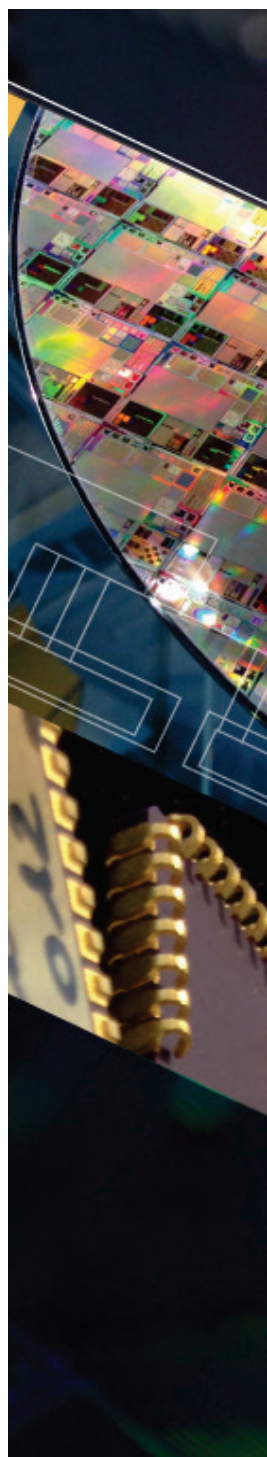
Distribution of integrated circuits with respect to providers in 2019

Distribution of integrated circuits per country and geographical area and per type of users

As expected, France is the country from which most institutions are working with CMP. Canadian and US institutions are also important. Then comes the one from Germany followed by Belgium, Russia and Sweden. This very wide community of users shows that CMP is really providing an original service that is interesting everywhere worldwide. Still France represents a very important contribution area as it will be highlighted in the next section.

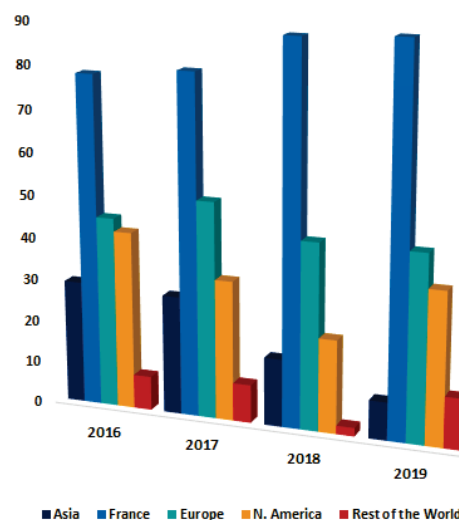
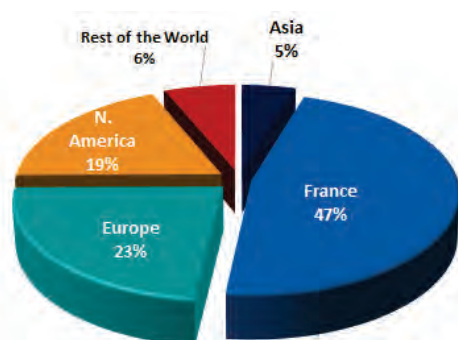
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Distribution of integrated circuits per country in 2019

In 2019 and with respect to previous years, the number of projects submitted by French institutions remains dominant but has returned below the 50%. In volume, the contributions from French institution is stable but in fact it is due to an increase number of contributions from the other parts of the world that produced the French percentage. Especially, more contributions from North America and rest of the World are reported, for both STMicroelectronics and ams technologies.



Distribution of integrated circuits per geographical area in 2019 and evolutions from 2016 to 2019

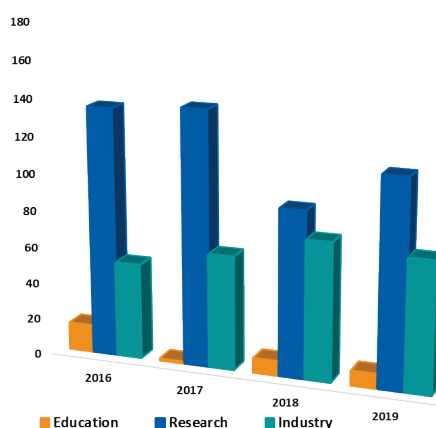
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Activity levels in the Asian region still declined this year like over the past five years, while the number of projects coming from European countries (except France) remain stable. Finally, 2019 shows a small increase in terms of projects submitted compared to 2018, but confirms a slight reduction in volume activity over the last 5 years. This trend, which began after the big 2007- 2009 period, when CMP was processing more than 400 projects a year, brings the CMP activity back to the previous period from 2001 to 2006. It is important to note that the total income remains stable over the years, the CMP user community migrating to more advanced technologies. In addition, the complexity of the technologies and the lead-time in designing, manufacturing and testing, impact significantly the quantity of circuits each research group can submit per year. Overall, CMP is facing in average a small decay in volume, compensated by the success of more advanced technologies.

Integrated circuits for academic research and education

In 2019, circuits for academic research represent 112 circuits (59% of total circuits) coming from 18 countries



Distribution of integrated circuits per user types from 2016 to 2019

Integrated circuits for industrial research purpose

71 industrial purpose circuits, 54 from France and 17 from foreign countries, were fabricated for 23 industrial companies (see the list in Appendix 2 on the CMP web site). This level of industrial participation represents 38% of the total number of circuits.

Low volume

In terms of small volume, 2019 was a good year, 32 low volume productions of integrated circuits for 18 Institutions, from fifty pieces to thousands of pieces or wafers have been fabricated. Please refer to Appendix 3 on the CMP web site for the complete list of low volume circuits fabricated.

New Institutions

22 Institutions (out of 82 all in all) participated for the first time in 2019. All the Institutions having submitted circuits from 1981 are listed in Appendix 4, appendices are available on the CMP web site <https://mycmp.fr>.

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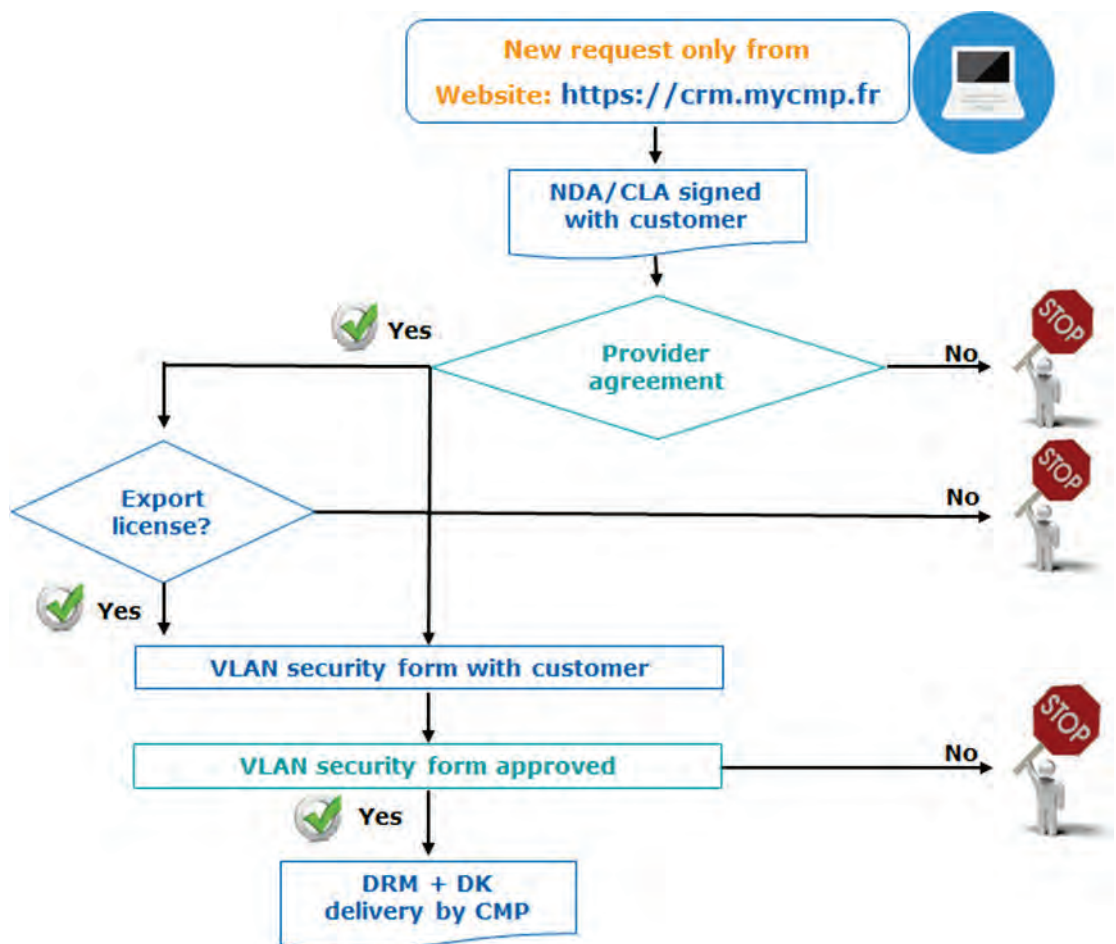
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Design Kits management and main data

CMP distributes, free of charge, the design kit for each technology, which includes technology files, and standard cell libraries for each specific CAD tool. In 2019, CMP handled 33 different Design Kits (corresponding to different technologies and different CAD tools), which were sent to customers upon signature of a Confidentiality and License Agreement.

Since February 2019, access to the Design Kit is given through myCMP, a new specialized web interface for MPW service management: end of December more than 260 institutions have request or updates of their DK via myCMP. This tool organizes access to all CMP services by unifying and interconnecting the various steps toward MPW participations. It serves as a secured stand-alone platform for communication and documents exchange along with an automated project status tracking.

First of all, customer need to create an account before making any request at the following address: <https://crm.mycmp.fr>. Once the account is validated, customer can place a request for DK. Hereafter is the flow chart for ST technologies Design Kits request.



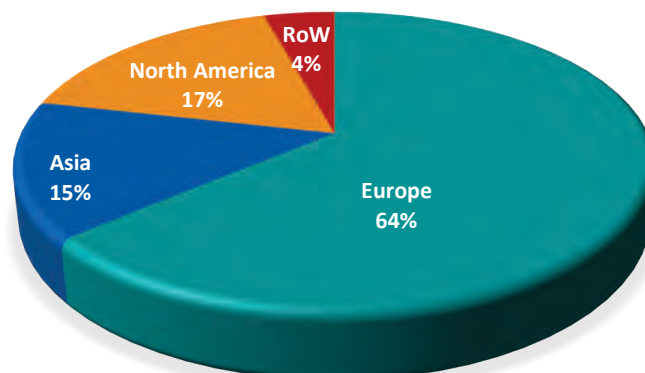
Flow chart: Design Kits request for most advanced STMicroelectronics technologies

Over 1200 customers, (academic centres and industrial companies) from 72 countries have already signed agreements and received Design Kits over the past 15 years.

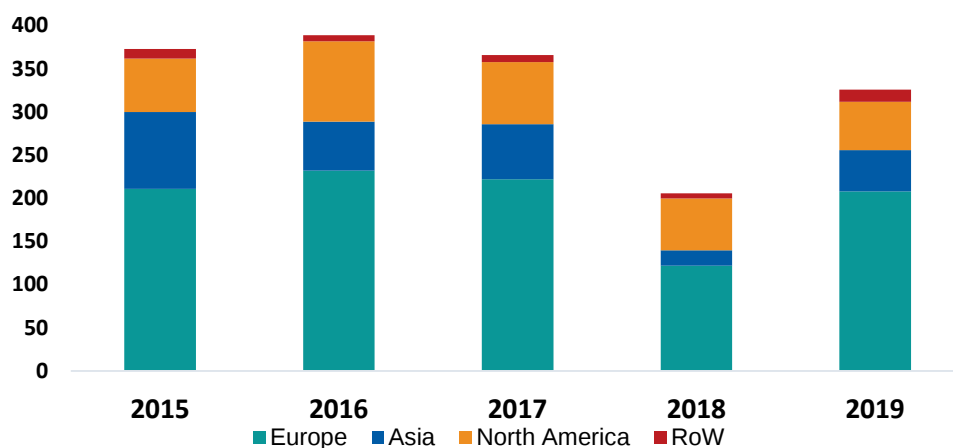
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In 2019, more than 330 Design Kits were distributed, according to the geographical distribution below. These data can be compared to previous years.



Worldwide Design kit distribution in 2019



Design kit distribution from 2015 to 2019

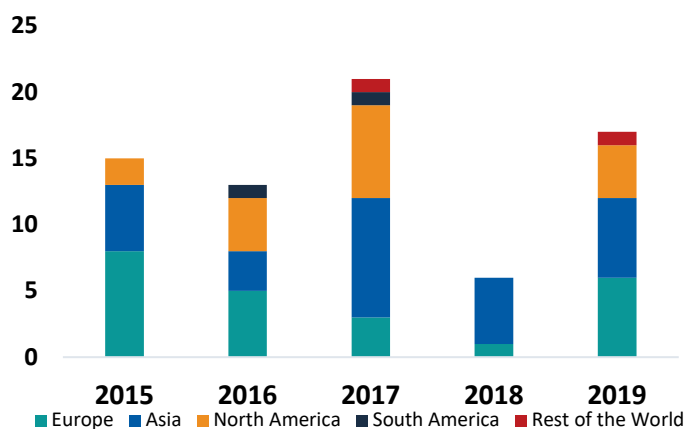
In 2018, a fairly significant decline has been observed in number of applications for ams Design Kits from the user community, mainly related to the end of the 0.18 μm technology distribution, also because the ams Hit-Kit in 0.35 μm technologies reached a maturity with no update between year 2017 and 2018.

In 2019, thanks to news services with ONSem and em μ electronics and due to reassuring news about the sustainability over several years of ams technologies, there has been an increase in demand for DK in mature technologies and new institutions have expressed interest for our extended portfolio. In the frame of Europractice, and more specifically with the cooperation between CMP and Fraunhofer IIS, it has been decided to extend the ams offer in 2020. The design-kit distribution and support will continue as done before, and MPW runs has been scheduled to offer prototyping and low volume productions services.

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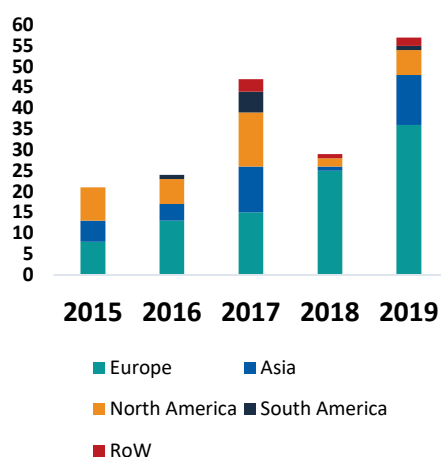
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Histograms below shows the distribution of Design Kits for new institutions per provider and geographical area from 2015 to 2019.

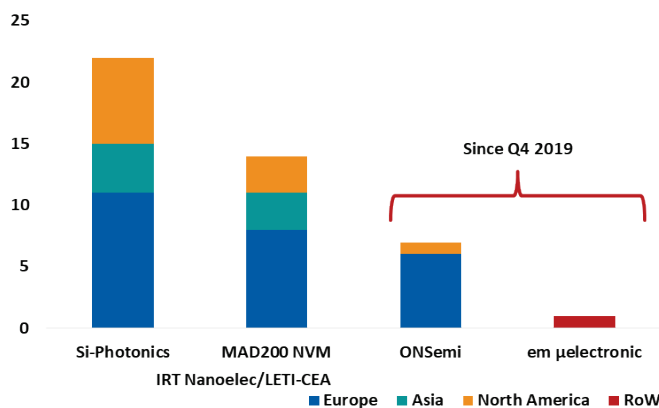


Number of new institutions which received ams design kits over the past 5 years

In 2019 CMP received an increasing number of requests for STMicroelectronics technologies, from new Institutions in Europe, confirming the interest of the European community for STMicroelectronics technology portfolio.



Number of new Institutions which received STMicroelectronics design kits over the past 5 years



Number of Institutions which received design kits in IRT Nanoelec/LETI-CEA, ONSem and em µelectronic technologies since the opening of each service through CMP

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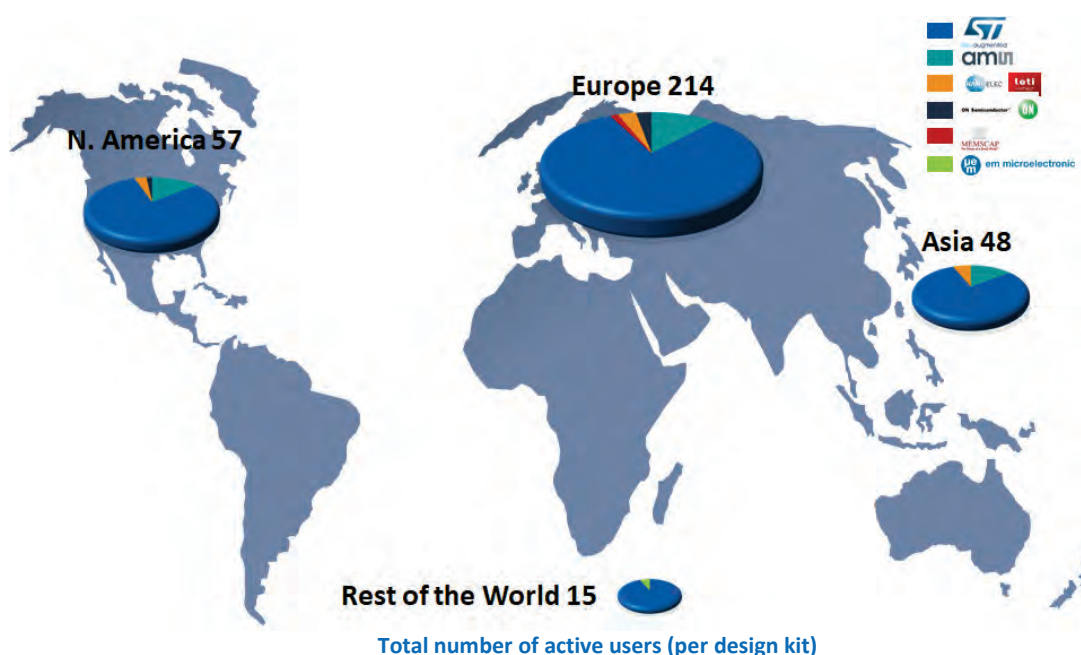
Globally the number of new Institutions which received design kits are:

- 17 new Institutions for ams with a total of 148 active Institutions
- 57 new Institutions for STMicroelectronics with a total of 360 active Institutions
- 24 new Institutions for IRT Nanoelec/LETI-CEA technologies with a total of 36 active Institutions (Si-Photonics and MAD200 NVM)

For the two news providers, which were introduced in the CMP portfolio in Q4 2019, we already received requests of access and the number of Institutions which received design kits are:

- 7 new Institutions for ON Semi technologies
- 1 new Institutions for em microelectronics

CMP active users mainly come from Europe (64%), North America (17%) and Asia (14%). Others customers come from India and Australia (4%).



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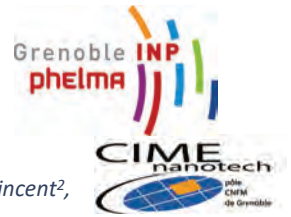
Focus

Novel practical lab for teaching in microelectronics systems: complete flow, from design to test, of an RF front-end at 2.45GHz

Sylvain Bourdel¹, Jean-Michel Fournier¹, Yannis Le Guennec¹, Ghislaine Maury¹, Florence Podevin^{1,2}, Laurent Aubard¹, Michele Potolan¹, Laurent Fesquet^{1,2}, Loïc Vincent², Robin Roland²

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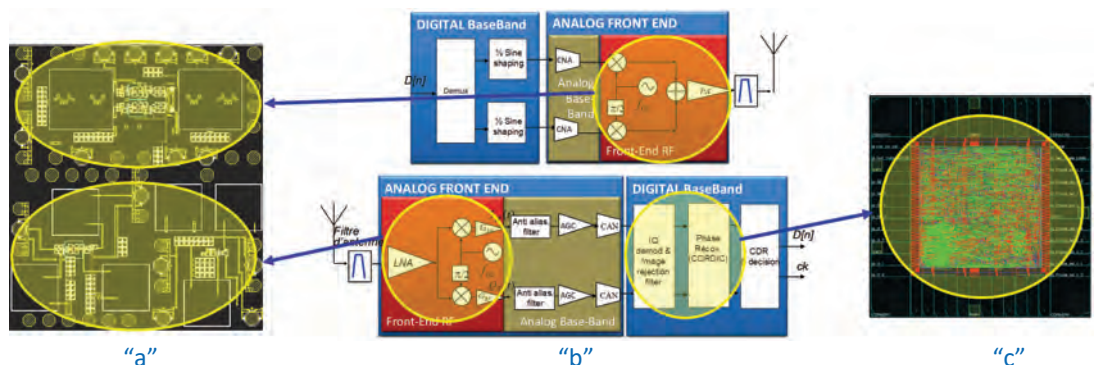
Context

Specific master degree per apprenticeship* in « Microelectronics and Communications » proposed by the Engineering School PHELMA from Grenoble INP group.

* 2 years after bachelor graduation, students with equivalent L2 degree can enter Phelma to pursue studies for 3 years until master degree. Apprenticeship in Microelectronics and Communications is proposed to 20 or so students a year.

Objectives

Gathering the students in apprenticeship (~20 students a year) in an industrial context in order to design and fully characterize a complete, complex, integrated system: a ZigBee transceiver. Students are organizing themselves in project teams to apply on a practical case the scientific theories they learnt during lectures, guided exercises and guided practical labs. They work on a specific CAD tool dedicated to microelectronics (Cadence, modelsim, ...) and benefit from the advice of professors with full expertise in communications, microelectronics design as well as the support of a professor in project management.



Legends

“a”: RF analog die including:

- transmitter front-end (IQ modulator and PA)
- Receiver front-end (LNA and IQ mixer)
- frequency synthesis (PLL)

“b”: System architecture of the TX-RX ZigBee

“c”: Digital die including:

- an IQ demodulator IQ with image rejection
- a Cordic decoder

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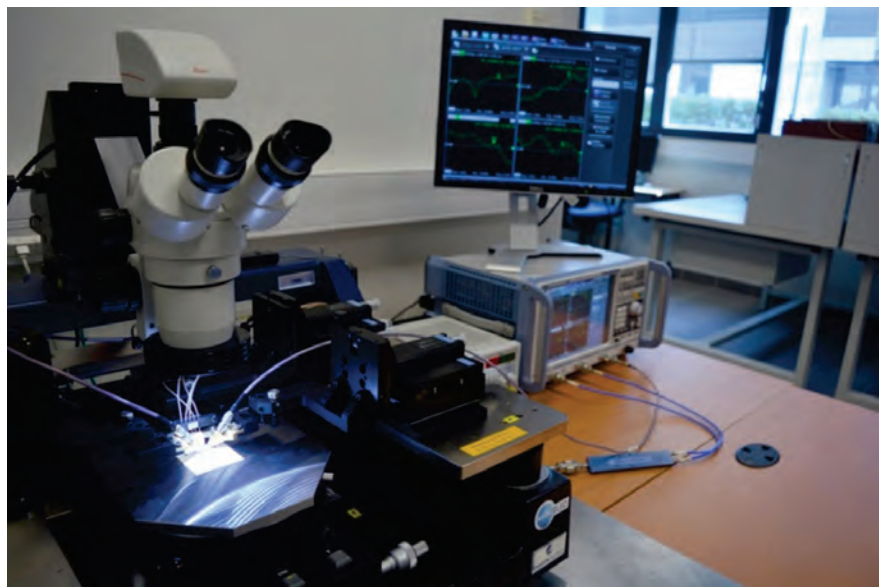


Step-by-step

1. System study, followed by all the students, with Simulink (12H under the supervision of an expert professor in communications)
2. Self organization of the project by the students, under the supervision of a professor in project management: students are working in duo, distribute their roles (one block design per duo, choose a project manager, etc ...), organize the agenda (milestones, design review, final report, etc ...)
3. Circuits design (72 h under the supervision of expert professors in microelectronics design + free slots), made at CIME
4. Circuits delivery (DRC clean, LVS clean, PLS performance OK)
5. Final assembly by the professors team
6. Fabrication through CMP – Grenoble (Circuits Multi-Projets®)
7. Test and characterization of the students packaged circuits during 20H of practical labs, followed by all the students: noise measurement (NF and phase noise), non-linearities (IIP3 et ICP1dB), system approach (QAM modulation), numerical tests (post-synthesis netlists applied to the students packaged circuit via FPGA), made at CIME

Tools (available at CIME – Nanotech)

- Illimited access to any Analog & Digital tools
- Cadence / Virtuoso, Calibre, Mentor
- Technology: 0,35µm of AMS (Austria Micro Systems)
- Test:
 - RF test boards
 - Probe test
 - VNA 8.5GHz
 - RF noise measurement
 - Signal generator and analyzer of MSK signals at 2,45GHz
 - Spectrum analyzer with phase-noise option
 - Test vectors generation (ATPG) through Tetramax
 - Test of circuits in package with an FPGA based tester



FPGA based tester

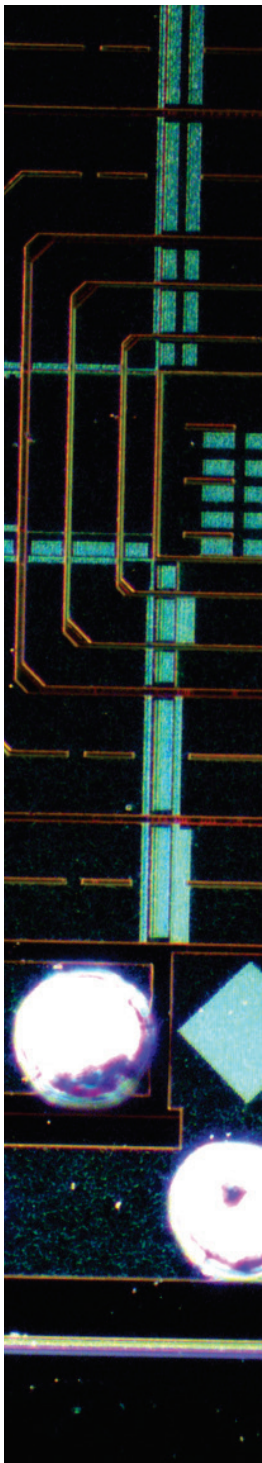
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CMP staff is working on the elaboration of a new platform, to make basic IPs developed by CMP community, available to other institutions who are working on the same technology. IPs portfolio available through CMP IP portfolio and IP sharing services through CMP will be made available in 2020.



IC Visual Inspection/Service Report on IC and project through CMP

Since this year CMP has launched a systematic visual inspection procedure with the objective to be engaged toward systematic improvements to the quality of services at CMP, for the benefits to users. An observation bench within an ISO Class 3 air quality environment allowing a safe visual inspection of integrated circuits, wafers and packaged dies has been built. This system consists of a precise camera for die scale picturing, a microscope for micrometer inspection (pad open, die edges, dust...) and a vertical laminar flow of clean air in which the observation will be carried out.

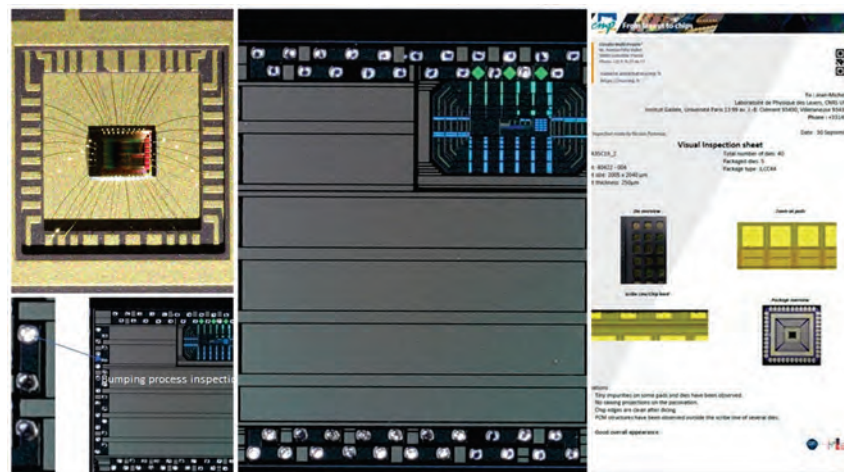


CMP staff doing visual inspection of the pad open of an IC manufactured and diced through CMP

Thanks to this installation, CMP is now able to offer a new set of services in complement to the current MPW services. These services consist to observe and control the quality of the incoming and outgoing dies, wafers or packaged dies received from the foundries and the subcontractors. Through this process, CMP also delivers a visual inspection report in order to give its users a detailed summary of the observation.

Moreover, high resolution photos of dies, wafers, and microscopic views of targeted areas (chip edges, pads passivation etc) can be made available on request (check for conditions function of the work request).

For each project, CMP will provide a visual inspection sheet in order to accurately show to the users what have been observed.



Visual inspection report

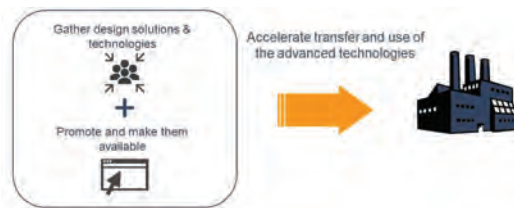
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A platform for power electronics prototyping services

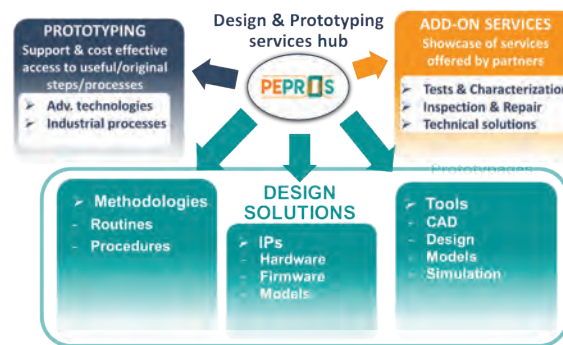
PEPROS (Power Electronics Prototyping Services) is a service platform launched by CMP dedicated to power electronics prototyping toward the R&D community. The objective of PEPROS is to facilitate the access and thus to accelerate the transfer and the use of disruptive technologies such as Smart Power ICs, advanced hybrid technologies etc. dedicated to power conversion.

CMP is currently working with academics, research organizations, start-ups, industrials and R&D departments to bring together design & technical solutions and breakthroughs in order to offer services based on their know-how, experience and research work.



Models, control & power blocks, simulation & design tools at component, converter and system level are about to be made available through PEPROS. Most of these IPs will be distributed to the users under licence agreement, free of charge depending on final use.

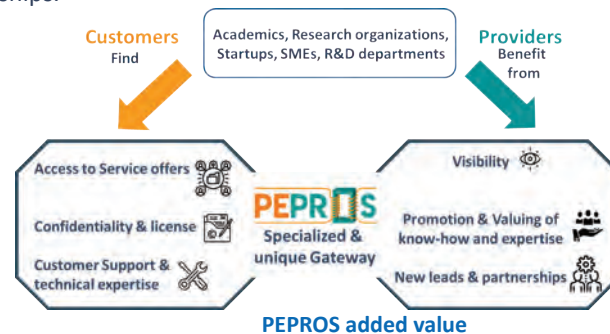
PEPROS offers also support and cost effective access to advanced technologies and industrial processes for prototyping of components, converters, packaging, interconnects, casing etc. Specific services from academics and industrials can be highlighted to give visibility to a design expertise, an important thesis, and a innovative IP, a characterization facility, a process or a methodology or a specific/original tools.



PEPROS services overview

A platform to narrow the gap between providers and users

The ambition of the PEPROS platform is to become a specialized and unique gateway making technically and economically possible the access to numerous power electronics technologies where users can find solutions and providers can find new leads building new research and industrial projects and partnerships.

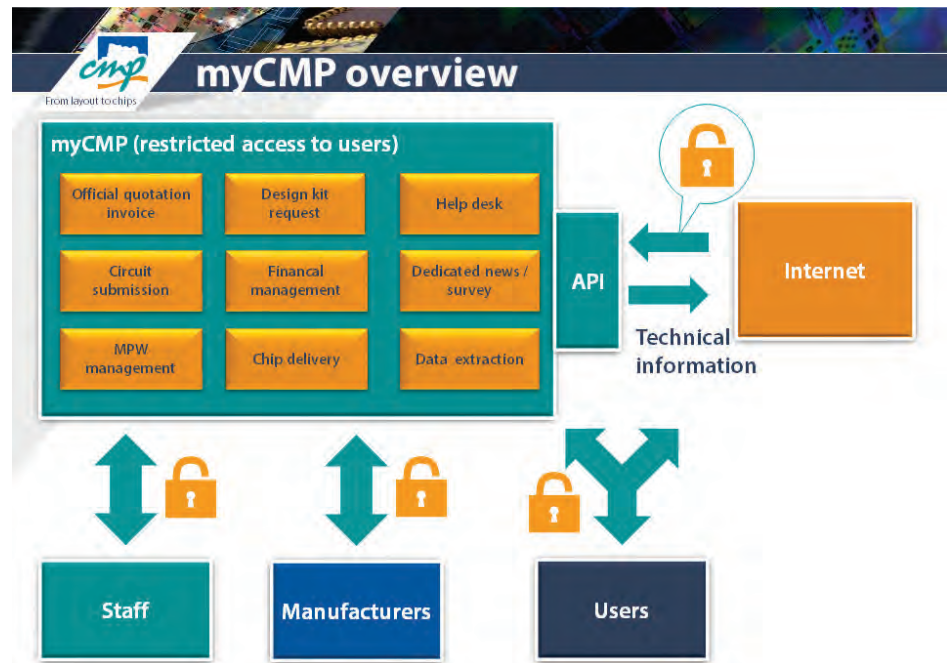


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myCMP Web application for MPW services management

myCMP is an all-in-one online interface between designers and CMP staff launched in January 2019. it aims to ease, record and concentrate all exchanges relative to a prototyping project and ensure the project management. The whole myCMP structure involves several modules as shown in the “myCMP at a glance” picture.



myCMP at a glance

We recall myCMP is available on line through the link <https://crm.mycmp.fr> and that tutorials on how to use it are available at <https://crm.mycmp.fr/documentation>

We are pleased to announce that the service is functional and fully adopted by the user community. Some key figures at this date :

- 246 registered institutions, with the following repartition : 120 Educational institutions, 73 Research laboratories and 53 SMEs.
- 283 NDAs have been requested and processed through the web-application
- 23 MPW runs have been conducted for 131 circuits.

So far, CMP received good feedback from users which helped to improve the tool. myCMP is evolving and will feature new modules in the coming year such as the integration of the technical design kit support center, IP requests, online quotations...and so on. Your feedback is still essential to ensure the development of the most efficient tool for the community and reach expectations.

myCMP has significantly improved the interaction between CMP staff and users by gathering all the activities and services maximizing record of information, full interactions among CMP services, legal, support, MPW management but also export licence, quotation, invoicing, news, update, reach out.

Please discover now some key features of myCMP and their added-value for project tracking:

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Design Kit request module

Requests of NDA can be followed step-by-step and major evolutions are systematically notified. myCMP is also automated to track the expiration date. It eases the renewal process and avoid delays in updating legal issues just before IC submission. Display boxes are colored according to the step the user is going through. Each box shows turnaround time, dates and gives access to all documents any time. All data are recorded, stored and remain accessible over time from both the user and CMP staff side. More steps can be necessary depending on the foundry requirements:

NDA

Estimated time : 10 days - Customer step

 NDA.pdf
 

 NDA_V1.pdf signed
 

Step opened on 04/11/2019 15:39 by Sylvaine EYRAUD
 Document not yet consulted by the client
 Step validated on 04/11/2019 15:40 by Sylvaine EYRAUD

DKLA

Estimated time : 20 days - Foundry step

 DKLA.pdf
 

 DKLA_V1.pdf signed
 

Step opened on 04/11/2019 15:40 by Sylvaine EYRAUD
 Document not yet consulted by the foundry
 Step validated on 04/11/2019 15:40 by Sylvaine EYRAUD

Status of typical NDA procedure

MPW shuttle run module

- From the MPW shuttle run menu on the left, reservations and circuit submissions can be managed. Each reservation and order are reviewed before validation by CMP staff. Then notification and email are sent for confirmation.

myCMP keeps the history of all reservations and orders and their status:

Run			
Dashboard	56	Inst_AC_ams_top_cell	A35R19_TEST
Make a reservation			Validated
My reservations	55	Inst_AC_top_cell	S28I19_TEST
Submit order			Validated
My circuits			

Table of submitted circuits through myCMP

- For higher clarity, users get real-time notifications of status and updates regarding their ongoing project such as data processing / in production / packaging:



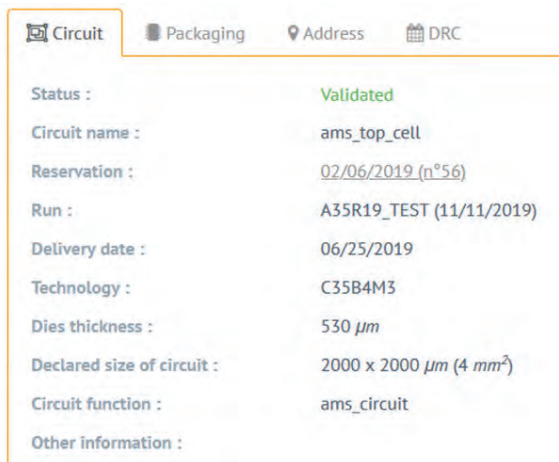
Project time table

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- With each order, a summary sheet gives the integrated circuit characteristics, additional services and specific customer requests. On DRC tab, an activity sheet is provided in addition to the DRC report and a follow-up of the different versions submitted to CMP. This is also an exchange platform for documents such as technical datasheets, waivers, hardcopies and so on:



Circuit	Packaging	Address	DRC
Status :	Validated		
Circuit name :	ams_top_cell		
Reservation :	02/06/2019 (n°56)		
Run :	A35R19_TEST (11/11/2019)		
Delivery date :	06/25/2019		
Technology :	C35B4M3		
Dies thickness :	530 μm		
Declared size of circuit :	2000 x 2000 μm (4 mm^2)		
Circuit function :	ams_circuit		
Other information :			

All relevant information related to a project at a glance

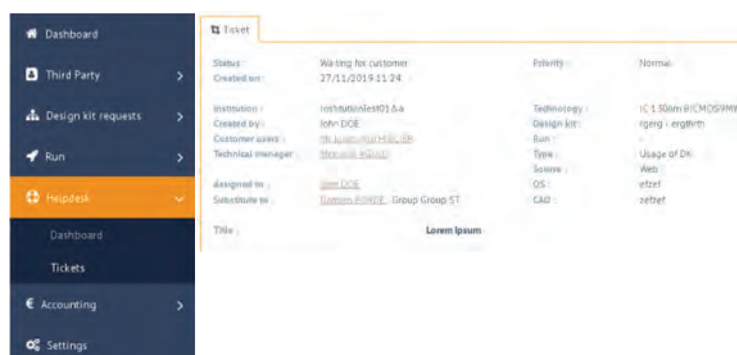
- myCMP introduces an integrated real-time chat which is appreciated for its spontaneity. It also quickens communication between the designer and the MPW manager.

Accounting module

Implemented beginning 2020 in myCMP, the accounting management module is designed to allow users having access to quotations and invoices of their projects directly in their accounts. With a valid account on myCMP, even without any valid NDA, a customer will be able to get an automatic budgetary quotation for their project on any technology offered by CMP. Then, with a valid NDA in place, it will be possible to request a formal quotation on the same interface. The accounting module gathers all the required informations for quotations and invoices from the MPW run menu in order to ensure data consistency. All emitted quotations and invoices are stored and remain accessible at any time.

Help desk module

- Also implemented beginning of 2020, the new support module is now integrated to myCMP. All features from the previous support module are preserved to warrant the same user experience. The main added-value features of this interface are single sign on, automatic verification of NDA status and direct communication with circuits in fabrication.



Ticket	Status	Waiting for customer	Priority	Normal
Created on:	27/11/2019 11:24			
Institution:	Institution test 01 Aa			
Created by:	John DOE			
Customer email:	john.doe@mycmp.fr			
Technical manager:	John DOE			
Assigned to:	John DOE			
Substitute to:	Thomas BOUTE, Group Group ST			
Technology:	IC150nm@CMP5PMW			
Design kit:	rgong - ergdgm			
Run:				
Type:	Usage of Dk			
Screen:	Web			
OS:	etzel			
CAO:	zetnet			
Title:	Lorem Ipsum			

The myCMP help desk interface

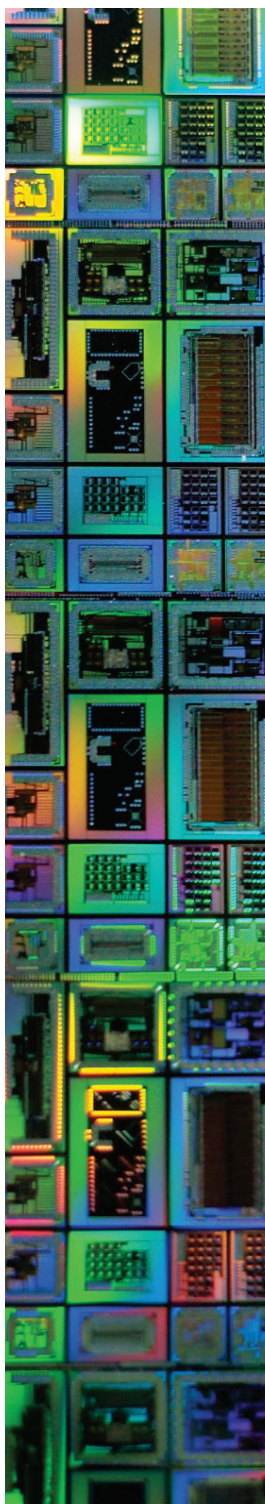
We hope you appreciate this new management tool to work with CMP and the enhancements it provides with this interaction.



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Nano 2022 / Important Project of Common European Interest (IPCEI)

CMP is pleased to announce its participation in Nano 2022 / IPCEI program, in collaboration with its historical partner STMicroelectronics and other academic and industrial contributors from the French and European microelectronics communities.



IPCEI is a European Research and Innovation Support Program published by the European Commission to support projects in strategic areas such as computing intensive, autonomous car or nanoelectronics. It offers the advantage of allowing public authorities to support participants beyond the research stage, also by funding the transition of innovations towards production.

In this project, called MPW-2022, the main objective of CMP is to enhance access to prototypes and small volume production in 28nm FDSOI technology for the European electronic ecosystem, by giving to the actors of the field the possibility to have a reliable access to this technology through regular manufacturing runs (2 and then 3 shuttle runs per year), with a more controlled and shorter lead-time fabrication.

Beyond the technical part itself, CMP will ensure, in conjunction with the key players of the IPCEI Nano2022 program, the setting of MPW dates, the monitoring of the run with information regularly disseminated to participants, the financial management of runs, the constitution of a complete report, for each MPW run, describing activity, participants, and distribution of contributions.

The expected technical and economic benefits are:

- First, with the MPW-2022 project, the 28FDSOI ecosystem will have a reliable, recurring and timely prototyping and small volume production tool. This will allow the players to secure silicon sourcing at early development stages and to have effective means of pooling.

If the first years 2 MPW will be guaranteed and subsidized. The objective is to achieve 3 MPW per year guaranteed and regular.

- With this prototyping resource that key players can count on, it is ultimately the financial means for the research and development of this whole ecosystem that will be able to benefit from the beneficial effects of the mutualisation. Public and private funders, using this tool, will be able to increase the number or size of objects developed at minimal extra cost.
- The entire sector will thus be able to gain in competitiveness on the R&D side.
- For CMP, the MPW-2022 project is an excellent vector for the development of the MPW activity in 28nm FDSOI from STMicroelectronics for a better sustainability given the difficulties encountered in recent years.

The IPCEI Nano2022 project also aims to fund CMP for the support activity associated with the implementation and use of STMicroelectronics Design Kits (DK), including IP access, tutorials and trainings.

At all stages of the interface and user relationship, CMP adapts its service to the technology offered and ensures the continuity of the service, according to the evolutions of the DK. All these technical activities are supplemented by legal management actions, confidentiality management, regularly updated to ensure the maintenance of security. Also, the STMicroelectronics/CMP partnership will be strengthened and CMP will be even more involved in the process of preparing and disseminating the new technologies that STMicroelectronics will decide to open in MPW. CMP will also implement IP sharing solutions in order to ease design and IP development among partners. Support will be focused on the following areas:

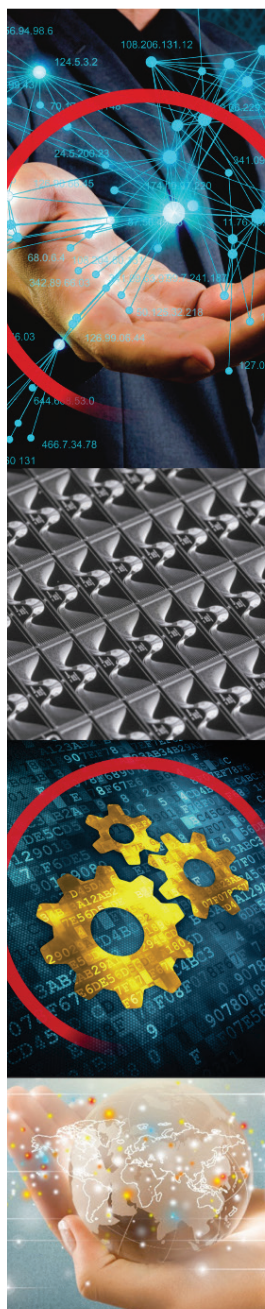
- Preparation of DK / Intellectual Property Management
- Promotion / training / tutorial / technical documentation
- Support for the installation and use of DK
- IP sharing and IP services to answer ecosystems basic needs.

The ambition is to meet the expectations of our users and to increase the number of projects at European scale in order to reach sustainability by the end of the program. The target is to meet the expectations of our users and to increase the number of projects at European scale in order to reach sustainability by the end of the program.

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MIRPHAB Pilot Line through CMP

In February 2018, CMP became the exclusive Broker of the H2020 MIRPHAB Pilot Line as well as a full member of the related MIRPHAB Consortium. Established at the beginning of 2016 as a 4-year project by leading RTOs and companies, the Pilot Line will run until the end of 2020 as an open platform for the prototyping and fabrication of Mid-Infrared (MIR) miniaturized chemical sensors, able to operate in both gas and liquids media.



Recent developments in integrated photonics components have paved the way to the miniaturization of MIR spectroscopy, otherwise confined to laboratory usage only, and nowadays used for real-time monitoring.

In addition to their reduced dimensions, these sensors enable in-situ and real-time detection, without pre-treatment or the requirement of additional equipment for the final detection. Therefore, MIR sensors are ideal candidates for integration in complex tools for on-line and direct monitoring of chemicals, and can be used for a wide range of fields such as the development of point-of-care devices for medical applications, the detection of pollutant gasses, and the control of the processes in pharmaceutical industry, to name a few.

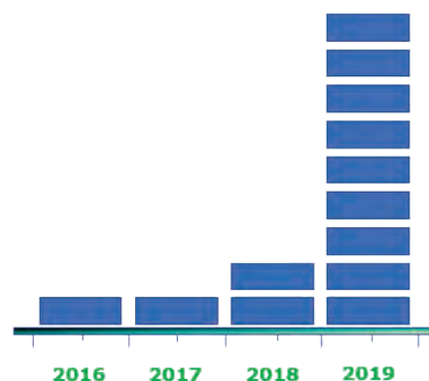
As the exclusive MIRPHAB Broker, CMP is particularly involved in the Consortium and handles the administrative, legal and financial relationships with the Pilot Line customers. CMP is notably in charge of the signature of the NDAs and the Service Supply Contracts, on behalf of the members of the Brokerage Activities Agreement (BAA). This year, the activity devoted to MIRPHAB has been reinforced with the arrival of Aurélien Nicolet at CMP.

One of the major issues faced by the MIRPHAB team was the difficulty to establish durable relationships with potential customers and to drive them into users of the pilot line, despite the possibility of financial support from the consortium – up to 80%. To tackle this issue, and in order to organize the follow up and help the end-users in defining & specifying their requests, CMP customized a **Customer Relationship Management (CRM)** tool to be used from the first contacts with potential users to the delivery of final prototypes.

In 2019, these increased efforts in the follow-up of potential customers, regular contacts and technical support have led to a growing number of companies willing to sign an NDA with CMP (on behalf of all MIRPHAB partners), highlighting the growth potential of MIRPHAB's business development in the coming months.



NDAs signed by CMP on behalf of all MIRPHAB partners

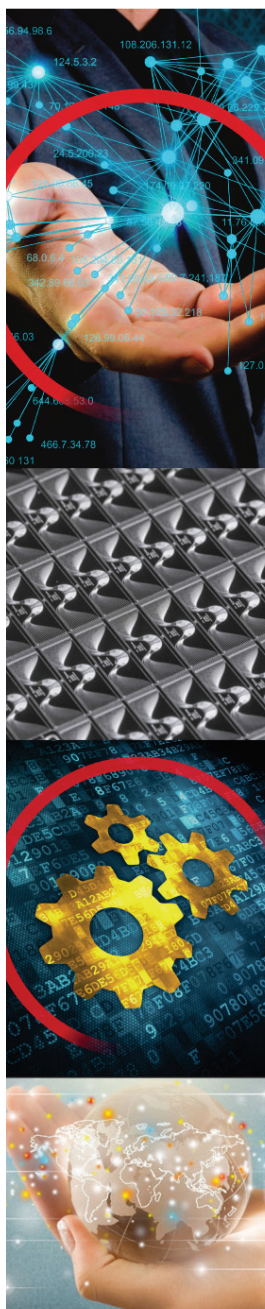


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<https://mycmp.fr/technologies/mirphab-pilotline.html>
www.mirphab.eu



As marketing and business development actions are still needed to reach the initial objectives set by the European Commission, CMP has been also actively involved in the promotion and dissemination activities of the Pilot Line. CMP represented MIRPHAB in several exhibitions in 2019.

Representation of the MIRPHAB Pilot Line at dedicated MIRPHAB booths with CMP staff	Representation of the MIRPHAB Pilot Line at CMP booths
Pittcon, 19-21 March 2019, Philadelphia, USA	DATE, 26-28 March 2019, Firenze, Italy
Sensors Europe, 10-11 April, Berlin, Germany	DAC, 3-5 June 2019, Las Vegas, USA
MedtecLIVE, 21-23 May 2019, Nuremberg, Germany	ECOC, 24-26 September 2019, Dublin, Ireland
Medica-Compamed, 18-21 November 2019, Düsseldorf, Germany	
Sensors USA, 20-21 November 2019, Santa Clara, USA	



MIRPHAB booth, Sensors USA 2019 from left to right
Coralie Gallis, CEA Leti, Jérémie Perret, CMP, Sergio Nicoletti CEA Leti

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<https://mycmp.fr/technologies/mirphab-pilotline.html>
www.mirphab.eu

Partners





EUROPRACTICE program: 2020 - Next Europractice eXtended Technologies and Services IC (NEXTS project)



H2020-project Next Europractice eXtended Technologies and Services
-NEXTS-

Since January 1st, 2019 and for the next 3 years, CMP is partner in the EUROPRACTICE program. The Consortium is composed of 5 partners : IMEC, UKRI-STFC, Fraunhofer IIS, CMP and Tyndall. The H2020-project is named NEXTS for Next Europractice eXtended Technologies and Services: "The access point for the future generation of electronic components and systems".

EUROPRACTICE Consortium support academic institutions and medium-sized companies with IC prototyping services, system integration solutions, training activities and possibilities for small volume production. In addition, the Consortium provides universities and research institutes with access to CAD tools.

During this year and the year before when setting up the project, there were several consortium meetings where the partners worked intensively for a coherent EUROPRACTICE offer. CMP joined the program not only as an increment to the existing service centers, but also adding complementary services and stimulating the cooperation and partnership. The first results of these continuous team working inside EUROPRACTICE has shown an increase of the service offer, a greater quality and a better visibility.

The EUROPRACTICE membership for the users is now also part of CMP identification. Each of the CMP user who has such membership is eligible to the price discount for MPW runs prototyping:
<https://mycmp.fr/technologies/price-list.html> / <https://europactice-ic.com/schedules-prices/>
On the other hand, CMP MPW run schedule is integrated into the EUROPRACTICE MPW run schedule.

Regarding the CAD tools used for design-kits distributed by CMP, there were in the past a full support from UKRI-STFC to provide to Universities the right CAD versions required by the design-kits. This collaboration between UKRI-STFC and CMP is naturally continuing in the frame of EUROPRACTICE. Trainings organized by CMP are also promoted and offered in EUROPRACTICE. Their visibility and access are increased. The training activity at CMP evolved and is now fully part of the offer. More information in this report at the Events section or at:
<https://mycmp.fr/services/training-courses> / <http://www.europactice.stfc.ac.uk/training>

This year, EUROPRACTICE organized National Seminars in different locations in Europe. CMP participated to those events together with the other partners. Other National Seminars are planned in 2020 covering other European locations.

For the PR and communication, different promotional material are coordinated inside EUROPRACTICE: Process flyers, Trainings booklet, Annual Report, exhibition posters, etc. CMP actively participate elaborating with the other partner the content of these material, as well contributing on their design. The same effort has been done by each partner for making the new EUROPRACTICE web site :<https://europactice-ic.com/>

The PR and communication collective work resulted on a great coherent visual promotional material.

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Promotional video of new extended EUROPRACTICE services



One of the tasks in EUROPRACTICE defined in the Project was to elaborate a promotional video in order to give more visibility to EUROPRACTICE and highlight the service's full potential. The main goal of this deliverable is to advertise and explain the EUROPRACTICE services. The video is available on the EUROPRACTICE web site. CMP enjoyed leading the task for this deliverable with the contribution of Romano Hoofman, from IMEC, Clive Holmes, John McLean from STFC, Thomas Drischel from Fraunhofer IIS and Ramsey Selim from Tyndall.

Events

In 2019 CMP was present during the following events, under the EUROPRACTICE umbrella:

- ISSCC: 17-21 February 2019, San Francisco, USA
- TRANSDUCERS: 24-26 May 2019, Berlin, Germany
- ESSDERC & ESSCIRC: 23-26 September 2019, Kraków, Poland
- EFECs: 19-21 November 2019, Helsinki, Finland

National Seminars

In 2019 CMP was present during the following EUROPRACTICE national seminars:

- 9 May 2019, FhG Munich, Germany
- 10 September 2019, ETH Zürich, Switzerland
- 12 September 2019, Tyndall Cork, Ireland



Representative people from the EUROPRACTICE consortium during National seminars 2019

Partners



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Events

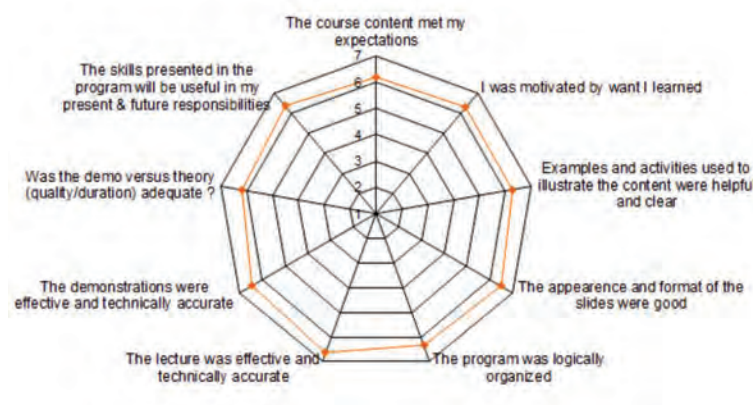
Training sessions

Started in 2015 in the frame of T2DO European Project and going on in the frame of Europractice, CMP is very happy to help its Users' community in getting skillfull designing ICs on its technology portfolio. We are now sorking on expending the training protfolio with additional trainings on various technologies available through CMP. Today, in the frame of EURO PRACTICE program, and to still improve our services, CMP works on a larger training offer.

CMP is planning four different training courses for 2020, sometimes with up to two sessions for the same course. Below is a preliminary schedule of these training courses:

Date	Training course	Location
February, 20 th 2020	Hardware-in-the-loop concepts and tools from Typhoon HIL 	Grenoble Institute of Engineering, Grenoble, FR
Mars or April 2020	Silicon Photonics "Si310-PHMP2M" technology, from CEA-LETI  	CIME Nanotech, Grenoble, FR
June or July 2020	28nm FDSOI technology from STMicroelectronics 	STM, Grenoble, FR
October 2020	55nm BiCMOS technology, from STMicroelectronics 	STM, Grenoble, FR
November 2020	28nm FDSOI technology from STMicroelectronics 	STM, Grenoble, FR

Up to now, two different training courses were offered to CMP users' community. Eight sessions have been held for the earlier training course, about ST's CMOS28FDSOI technology. Additionally, CMP recently opened a new training course, based on ST's BiCMOS55 node.



These training courses attracted students, professors, researchers and engineers from all over the world, gathering a total of 165 participants!

Below is an extract of the results given by attendees from latest training session:

The feedback surveys testify of these top-quality programs, with an overall score of more than 18/20.

CMP users will receive an invitation by email as soon as booking is open for the different training courses. **The registration will be accessible for institutions with NDA and/or tool license agreements in place for the corresponding technology.**

More information: <https://mycmp.fr/services/training-courses/>

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Isabelle AMIELH
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cmp-trainings@mycmp.fr



Users' annual meeting

The 2019 users' meeting, open to every person from academia or industry, using or interested in the CMP services, took place on February 7th at Institut de Physique du Globe de Paris (IPGP).

The meeting was focused on the presentations of CMP MPW and packaging services together with the participation of our partners, especially with the following presentations:

- Imaging Technologies at STMicroelectronics, Sara Pellegrini, STMicroelectronics
- EM Ultra low power technology services through CMP, Christian Terrier, em microelectronics
- ON Semi technology services through CMP, Gerhard Koops, ON Semi

Presented slides (PDF) of previous years of invited speakers are available at : <https://mycmp.fr>

90 people attended the meeting coming from 54 Institutions: Academia: 53 (47 French, 6 Foreign), Industry: 37 (29 French, 8 Foreign).



User's meeting

In 2020, the users' annual meeting will take place on January 30th, again at Institut de Physique du Globe de Paris (IPGP).

In addition with a complete review of up-to-date CMP MPW and packaging services, the following topics will be discussed:

- New technology services through CMP
- Photonics ICs
- New developments @ CMP

Thank you for your visit, feel free to contact us for any request.

More information: <https://mycmp.fr>

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Contact:

Romain VERLY
MPW Runs / ST 130 & 65nm
Romain.Verly@mycmp.fr

One-Day introduction to IC prototyping by CMP

CMP will organize in Pôle MIGREST, École d'ingénieur Télécom Physique à Strasbourg on Thursday, February 6th, 2020 the fourth day of introduction on integrated circuit (IC) prototyping - fundamental steps toward manufacturing. CMP intends to create an annual session to address the educational community in different cities in France. The first issue held on Paris in 2016, the second held in Montpellier and the third one held in Lyon St Etienne.



Novice designers (Engineers, Master2 and PhD students) will learn more on how to prepare a design toward its prototyping and how to interact with the MPW providers. This course is open to everybody involved in microelectronic design, academics or industrial, planning to submit their first IC design for prototyping.

The most important goal of this Introduction day is to raise awareness about important steps in IC prototyping (from the technology choice to the chips packaging) through a Multi-Project Wafer (MPW) services. Design aspects or technical descriptions of manufacturing processes will be discussed only briefly.



CMP staff interacting with registered participants



We thank the CNFM who helps us with the dissemination of the call and graciously offers us its premises.

More information: <https://mycmp.fr>

Participation to exhibitions

CMP exhibits in major conferences in Europe and US for more than 20 years. With the introduction of new technology services (advanced packaging, Photonics, Smart Power), to broaden its visibility and meet potential new users, CMP targets other important events, in complementary application fields.

In 2019 CMP has presented its activities and services during the following events:

- DATE, 26-28 March 2019, Firenze, Italy
- ECTC, 29-30 May 2019, Las Vegas, USA (Booth #520)
- PCIM, 7-9 Mai 2019, Nuremberg, Germany (Booth #7-252)
- DAC, 3-5 June 2019, Las Vegas, USA (Booth #644)
- ECOC, 24-26 September 2019, Dublin, Ireland (Booth #405)
- European MEMS and Sensors Summit, 19-21 September 2019, Grenoble, France



CMP booth at different conferences in 2019

Forecasts for 2020 events are:

- Forum de L'électronique, 11-12 February 2020, Grenoble, France (Booth #E107)
- DATE, 10-12 March 2020, Grenoble, France
- PCIM, 5-7 May 2020, Nuremberg, Germany (Booth #7-165)
- ECTC, 26-29 May 2020, Lake Buena Vista, USA (Booth #120)
- Symposium de Génie Electrique, 30 June – 2 July 2020, Nantes, France
- DAC, 20-22 July 2020, San Francisco, USA (Booth #1311)
- ECOC, 21-23 September 2020, Brussels, Belgium (Booth #191)
- European MEMS and Sensors Summit, 22-24 June 2020, Grenoble, France (Booth #14)

Have a look at the upcoming shows - if you're around, take out a little time and come visit us!

<https://mycmp.fr/>

Contact:

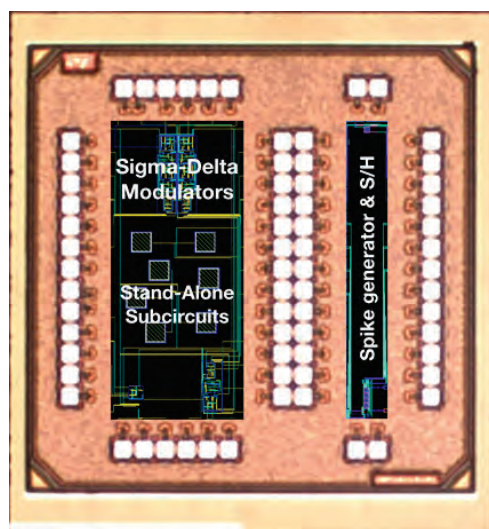
Isabelle AMIELH
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Examples of manufactured ICs through CMP

The Circuit Gallery at CMP is a place where CMP users can exhibit their designs and prototypes with pictures, project description, test results and publications. This Gallery is a showcase where CMP users can promote their research and development work to the community.

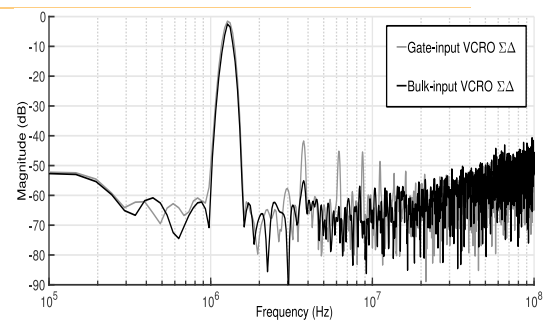
Body-Input Circuits with Enhanced Linearity
Instituto de Microelectrónica de Sevilla, IMSE-CNM
(CSIC/Universidad de Sevilla), Spain
<http://www.imse-cnm.csic.es>

CMP run ref.: S28I19_1
Process Technology: ST 28nm FD-SOI CMOS



Circuit name: VCOsDM
Contact Name(s): Luis Camuñas-Mesa, Jose M. de la Rosa
E-mail(s): [camunas, jrosa]@imse-cnm.csic.es

Introduction / Application: The main objective of this research work is to exploit the use of enhanced body effect of ST 28nm FD-SOI CMOS technology to improve the performance of analog and mixed-signal circuits (integrated in the left part of the chip) in terms of linearity, compared to the use of bulk CMOS processes. The chip includes also a pulse generator circuit (right part) for building a tunable spiking neuron which can generate spikes with controllable shape.



This will be used for implementing Spiking Neural Networks (SNNs) with STDP learning capabilities. Finally, the chip includes also a sample-and-hold circuit for characterization.

Description / Results: As stated above, several circuits are integrated in this test chip and used as a proof of concept to test the benefits of the ST 28-nm FDSOI CMOS technology in terms of enhanced body effect to improve the linearity of some analog and mixed-signal circuits, such as Voltage-Controlled-Ring Oscillators (VCROs) and their application to design Analog-to-Digital Converters (ADCs). A simulated output spectrum of a 2nd-order VCO-based modulator is depicted by showing the linearity improvement.

Publication references / link to web site: J. Ahmadi-Farsani and J.M. de la Rosa: "Bulk-Input VCO-based Sigma-Delta ADCs with Enhanced Linearity in 28-nm FD-SOI CMOS." Proc. of the 2019 IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, May 2019 (DOI: 10.1109/ISCAS.2019.8702810)

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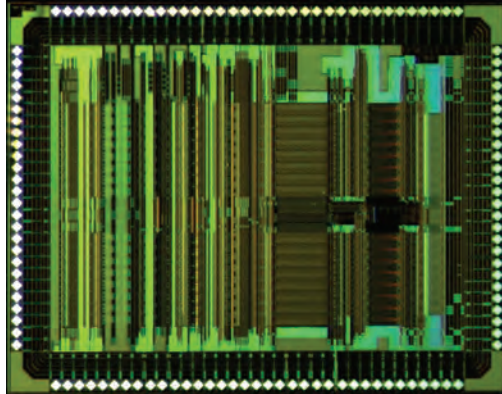
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A readout chip dedicated to small animal PET imaging
DRHIM IPHC IN2P3 CNRS Université de Strasbourg, France
<http://www.iphc.cnrs.fr>

CMP run ref.: A35C18_4

Process Technology: CMOS 0.35 μm



Circuit name: imotep2

Contact Name(s): Rachid sefri & Xiaochao Fang

E-mail(s): rachid.sefri@iphc.cnrs.fr

Introduction / Application: PET imaging, SiPM electronics readout.

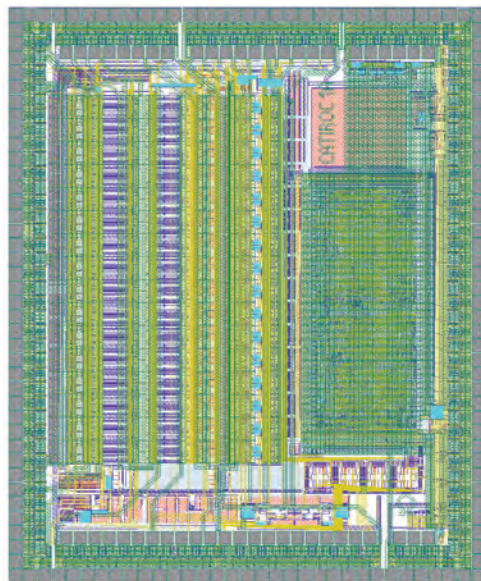
Description / Results: This Silicon photo-multiplier front-end chip embeds 16 parallel channels featuring energy measurement and time stamping in $3.7 \times 4.3 \text{ mm}^2$. Each channel has a dynamic input, ranging from 150fC to 2.7nC charge from photo-detectors. The analogue chain consists of a low noise current mode preamplifier, an integrator, a gain corrector compensating the photo-multipliers gain variation, a CR-RC shape reducing out band noise and an analogue memory. The arrival time reference is generated by a current mode comparator. The time stamped in each channel is provided by a reference time unit build around a DLL and a coarse time counter running at 80MHz, the time bin size is 25 ps. The readout is continuous and transfers are performed via a multiplexed analogue output for the energy and a serial digital output for the time.

CATIROC1A

Omega, Ecole polytechnique, Palaiseau, France
<https://portail.polytechnique.edu/omega/fr>

CMP run ref.: SA35S18_1

Process Technology: ams0.35 μm



Circuit name: CATIROC1A

Contact Name(s): Conforti Selma

E-mail(s): conforti@omega.in2p3.fr

Introduction / Application: Front-end electronics for photomultipliers read-out; Multichannel ASIC; System on chip; Autotriggering; Neutrinos experiments.

Description / Results:

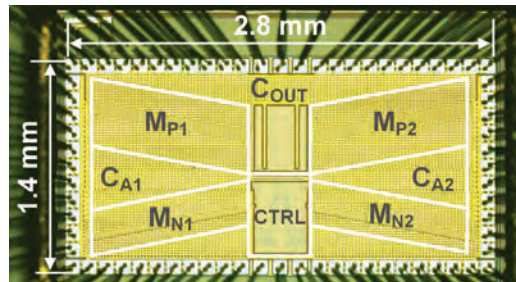
Catiroc1 is a 16-channel front-end ASIC designed to readout photomultiplier tubes (PMTs). The concept of the ASIC is to combine an auto-trigger chip to 16 PMTs to obtain an autonomous macro-cell. The 16 channels are totally independent and the trigger starts the charge and time measurements which are then converted and stored. Only the hit channels are read out. The time measurement is done by a 26-bit counter at 40 MHz and a Time to Amplitude Converter for the fine time, giving a resolution of 200ps RMS. The charge measurement is done by a preamplifier followed by a shaper with variable shaping times. Charge and fine time values are converted by a 10 bit ADC.



Bi-directional Wireless Power Transceiver
University of Macau, Macau, China
<http://www.amsv.um.edu.mo>

CMP run ref.: A35R17_1

Process Technology: ams 0.35 μ m RF
C35B4M3

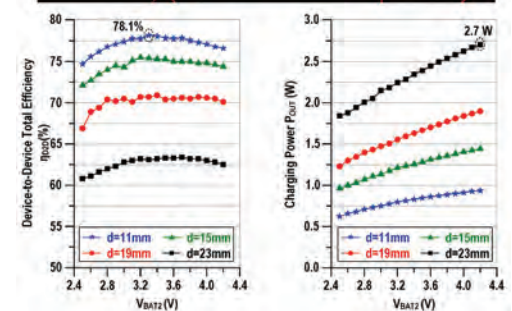
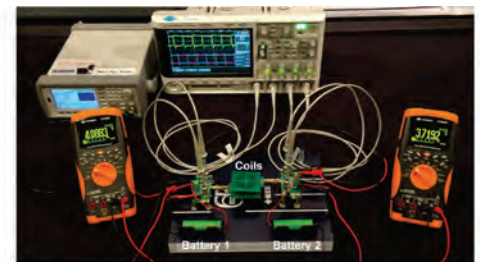


Circuit name: Wireless Power TRX
Contact Name(s): Fangyu Mao, Yan Lu
E-mail(s): YB57434@um.edu.mo,
yanlu@um.edu.mo

Introduction / Application: Bi-directional wireless charging via inductive coupling has become a popular subject as it enables the flexible power reallocation among different portable objects. To transfer the power from one electronic device to another wirelessly and efficiently, a reconfigurable cross-connected wireless power TRX was implemented on this chip.

Description / Results: The presented reconfigurable wireless power transceiver can be configured to transmitter (TX) mode and receiver (RX) mode with most of the hardware being reused, reducing the cost and shrinking the system size. With the cross-connected structure in both TX and RX modes, and the adaptive optimum switching timing control, high power efficiency is achieved. Operating at 6.78MHz, a peak total power efficiency of

78.1% is realized when transmission distance is 11mm. The peak output power is 2.7W with a total power efficiency of 62.7%.



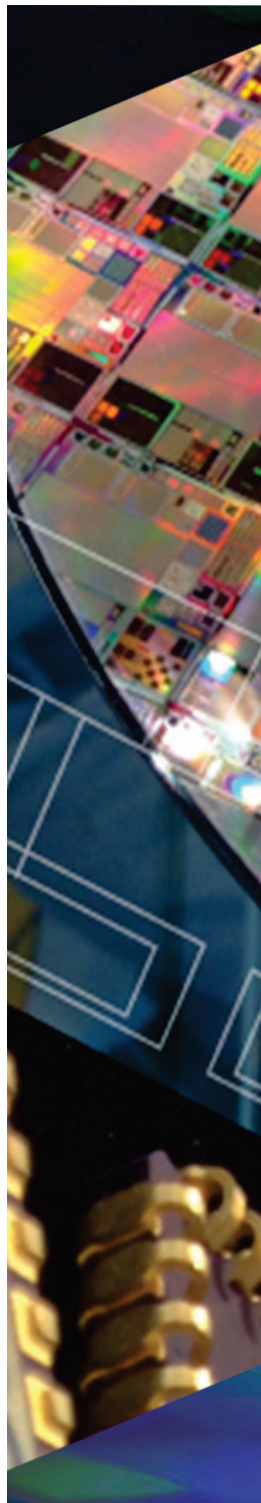
Publication references / link to web site: F. Mao, Y. Lu, and R. P. Martins, "A Reconfigurable Cross-Connected Wireless-Power Transceiver for Bidirectional Device-to-Device Wireless Charging," in IEEE Journal of Solid-State Circuits, vol. 54, no. 9, pp. 2579-2589, Sept. 2019.

F. Mao, Y. Lu, S.-P. U, and R. P. Martins, "A reconfigurable cross-connected wireless-power transceiver for bidirectional device-to-device charging with 78.1% total efficiency," 2018 IEEE International Solid - State Circuits Conference - (ISSCC), San Francisco, CA, 2018, pp. 140-142.

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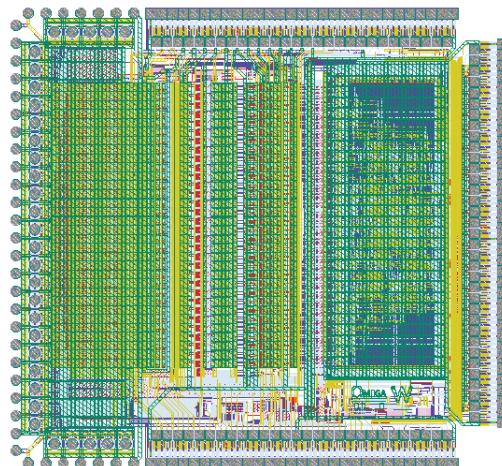
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Petiroc2b

OMEGA/WEEROC, PALAISEAU, France
<https://portail.polytechnique.edu/omega/fr>

CMP run ref.: SA35S18_1
Process Technology: ams 0.35 μ m S35D4M5



Circuit name: petiroc2b
Contact Name(s): Nathalie Seguin-Moreau (for academic use), Julien Fleury (for industrial use)

E-mail(s): nsmoreau@in2p3.fr, or
julien.fleury@weeroc.com

Description / Results: Petiroc2b is a 32-channel front-end ASIC designed to readout Silicon Photomultipliers (SiPM) for particle time-of-flight measurement applications and for any application that requires both time resolution and precise energy measurement.

It combines a very fast (GHz) and low-jitter (50 ps) trigger with accurate charge and time measurements which are digitized internally thanks to two integrated 10-bit ADC. A multiplexed charge output is also available as well as the 32 trigger outputs.

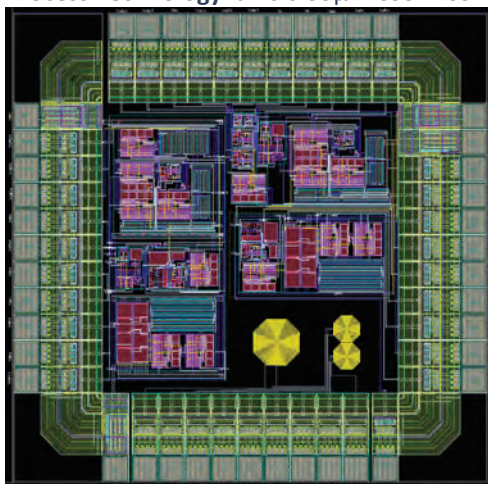
An adjustment of the SiPM gain is possible using a channel-by-channel input DAC.

The power consumption is 6 mW/channel.

Implementation of functional blocks

C2N, Palaiseau, France
<https://portail.polytechnique.edu/omega/fr>

CMP run ref.: A35C18_2
Process Technology: ams 0.35 μ m C35B4C3



Circuit name: CI_2018Mai_44
Contact Name(s): Ming ZHANG
E-mail(s): ming.zhang@u-psud.fr

Introduction / Application: In many applications, we need to generate a reference signal with a constant frequency as well as a constant amplitude whatever is the working condition. Among the possible signal waveforms is a sinusoidal one.

Description / Results: Usually the desired signal can be restored from the incoming signal. However, the amplitude can be hardly assured to be always constant even though the frequency is more likely to be intact due to the imperfection of the real world. This is why we need an automatic gain control circuit. Different functional blocks are designed and implemented in the chip with different constraints in terms of the frequency, tracking speed, stability.

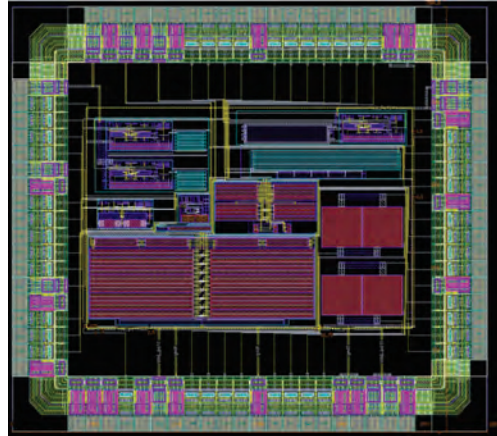
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Low noise preamplifier for SCM
Laboratory of Plasmas Physiques (LPP) / CNRS, Palaiseau, France
<http://www.lpp.polytechnique.fr>

CMP run ref.: A35C18_4
Process Technology: ams 0.35 μ m C35B4C3



Circuit name: PAFMLPP
Contact Name(s): Fatima Mehrez
E-mail(s): [mailto:j](mailto:jmailto:fatima.mehrez@lpp.polytechnique.frea)
<mailto:fatima.mehrez@lpp.polytechnique.frea>
n-denis.techer@lpp.polytechnique.fr

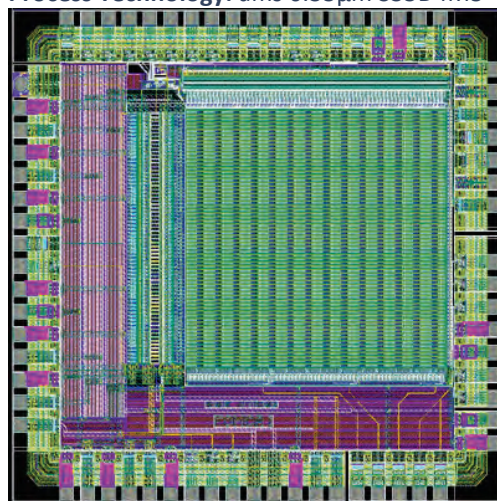
Introduction / Application: LPP provides very sensitive search coil magnetometers (SCM) that measure

variations of the magnetic field in space. Their sensitivity is of the order of magnitude of few tens of pT/Hz^{1/2} @ 1 Hz. So far, front end electronics used after these detectors are composed of discrete electronic components qualified for the use in space. This chip is part of the continuous R&D that aims to provide an integrated circuit keeping pace with the sensitivity of the detector while reducing the mass, volume, and consumption of the front-end electronics.

Description / Results: A first ASIC was developed in the same technology (ams 0.35 μ m). Some improvements in terms of stability, noise, gain and consumption. Are under study. This chip is a one channel ASIC dedicated to test these improvements. It contains two voltage amplifiers and a single-ended to differential signal converter besides a voltage reference and a current generator

Integrated Streak Camera With on Chip Averaging
ICube laboratory (CNRS – University of Strasbourg), Strasbourg, France
<http://icube.unistra.fr>

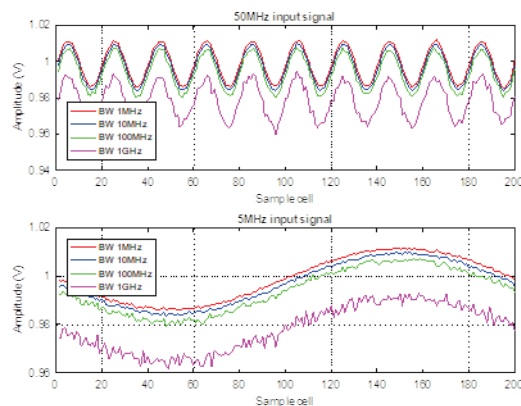
CMP run ref.: A35S18_1
Process Technology: ams 0.35 μ m S35D4M5



Circuit name: FOMCA1
Contact Name(s): J-B Schell, Wilfried Uhring

E-mail(s): jbschell@unistra.fr,
wilfried.uhring@unistra.fr

Introduction / Application: The streak imaging approach is the sampling of just a single spatial line of the scene per unit of time, resulting in a spatiotemporal image which can reach a time resolution about 100 times better than the framing mode. Thus, a temporal resolution better than 1 ns can be achieved while the fastest ultrafast video imager offer a temporal resolution around 100 ns. The drawback of a such high bandwidth performance is the noise of the system that increases with the cut-off frequency. In the case of a repeatable input signal, we demonstrated that the noise rejection can be adjust independently of the effective bandwidth of the system. Moreover, the readout time (a few Hz) is not limiting the event repetition rate.



Description / Results: The readout bottleneck can be circumvented by a high repetition rate on chip averaging. By controlling the voltage of the sampling cell, it is possible to adjust the

bandwidth. The circuit FOMCA1 is composed of a vector of 64 photodiodes, each connected to a sample line of 200 cells. The figure shows the results of a sample line for two input signals (5MHz and 50MHz) with different bandwidths in the range of [1MHz; 1GHz]. The resulting signal-to-noise ratio is more than 10 times better with an acquisition time of only 20 μ s.

Publication references / link to web site: W. Uhring, J-B.Schell, L. Hébrard, "Integrated Streak Camera With on Chip Averaging for Signal to Noise Ratio Improvement", IARIA SIGNAL 2019, Greece, vol.ISBN 978-1-612008-71, pp.33-36, Jun. 2019.

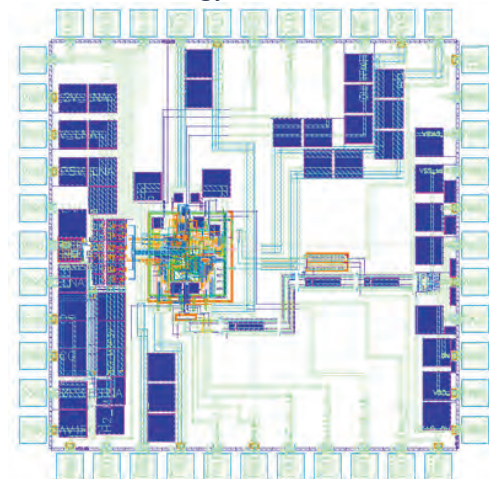
High HR II-delayed 5-PATH MIXER

RFICLAB Grenoble France

<https://rfic-lab.univ-grenoble-alpes.fr/>

CMP run ref.: S28I19_1

Process Technology: ST 28nm CMOS28FDSOI



Circuit name: NPAThone

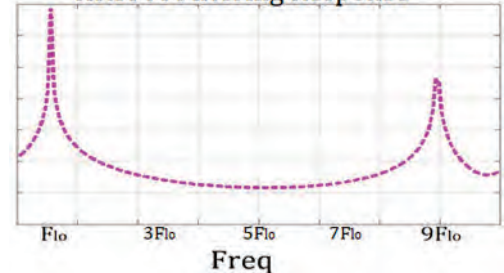
Contact Name(s): Sylvain BOURDEL

E-mail(s): sylvain.bourdel@univ-grenoble-alpes.fr

Introduction / Application: This circuit consists on a full differential 5-path mixer for low power and wideband applications. The N—path mixer structure achieves a selective RF filtering that can be tuned accordingly to the LO frequency. However, its output suffers from the presence of harmonics due to mixing. By using an RF differential signal and a π -delayed driving signals, the proposed circuit presents the same harmonic rejection than its 2N-path counterparts while reducing by 2 the frequency

of operation and showing a reduced number of differential gain stages and switches.

HR5PM Filtering Response



Description / Results: The proposed architecture improves harmonic rejection without increasing the complexity compared to conventional LNA-first receivers. This 5-path mixer rejects up to the 8th harmonic with only 3 differential gain stages whereas only the 6th harmonic would be rejected with conventional topologies having the same number of amplifier stages. The RF bandwidth considered is from 300MHz to 2.4GHz. The even harmonics are removed from the frequency spectrum of $e_{f(t)}$ thanks to the differential architecture. The other harmonics are rejected about 73dB, 78dB and 67dB for the 3rd, 5th, and 7th harmonics respectively.

Publication references / link to web site: A. A. Shakoush, E. Lauga-Larroze, S. Subias, F. Podevin, T. Tarris, S. Bourdel, "Low Complexity Architecture of N-Path Mixers for Low Power Application", Proc. 17th IEEE Int. New Circuits and Systems Conf. (NEWCAS), Munchen, Germany, June 2019

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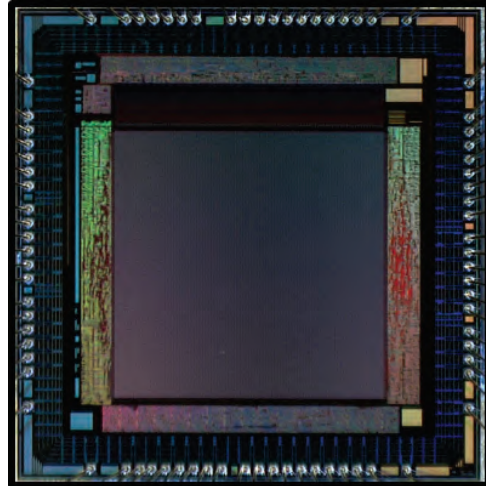
CMOS Image Sensor with Two-Tap Pixel-Wise Coded Exposure for Compressive Sensing

University of British Columbia, Vancouver, B.C., Canada

<https://www.ece.ubc.ca>

CMP run ref.: ICMBCUBC

Process Technology: ams 0.35 μ m CMOS Opto



Circuit name: CMOS Image Sensor

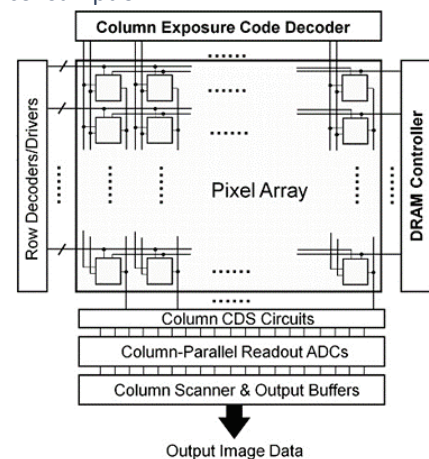
Contact Name(s): Yi Luo and Shahriar Mirabbasi

E-mail(s): luoyikey@ece.ubc.ca,
shahriar@ece.ubc.ca

Description / Results: The proposed CMOS image sensor consists of variety of functional blocks. The row decoder block performs row-by-row scanning to provide reset, charge transfer, and readout signals to the pixel array. The DRAM controller is a row scanner which sequentially selects a row of pixels to enable their exposure codes refreshment. During sensor readout periods, the pixel array is read out using a correlated double-sampling (CDS) scheme realized by column-based CDS circuits. Before reaching to a column scanner to output the final image data, pixel output signals are digitized to corresponding digital format through an analog-to-digital convertor (ADC) placed in each column. The fabricated image sensor chip contains 192 $\times$ 192 pixels with a pixel pitch size of 17.2- μ m and a fill factor of 35.2%. The chip is powered by two separately regulated 3.3V power sources – one supplies for analog circuits and the other for all digital control modules. In a dark environment, the pixel dark current is measured as 1.36 fA. The lowest achievable detection limit of a pixel is 10.8 nW/cm². By calculating the mean of the standard deviation of all pixel outputs, the extracted pixel and column fixed-pattern noise (FPN) are 0.19%

and 0.26%, respectively. The prototype camera equipped with the proposed CMOS image sensor experimentally demonstrated single-frame pixel-wise coded exposure in both spatial and temporal domains. Operate at 10fps, the image sensor is exposed to scene for long period and improves SNR in recovered images. In each frame, as pixel readout is not required until coded exposure is accomplished, CS are naturally applied during the exposure period and the image sensor follows a conventional reset-exposure-readout operation flow

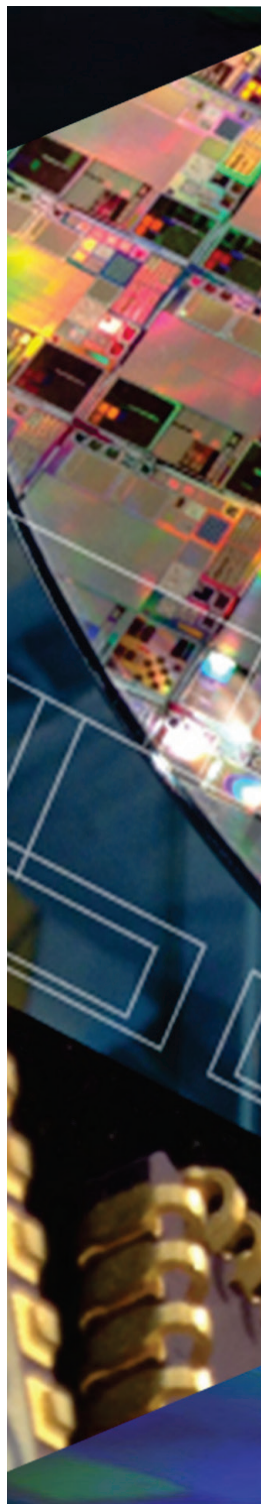
Introduction / Application: Compressive sensing (CS) is one of widely applied theories in computational imaging paradigms. Currently, pixel-wise coded exposure is developed to demonstrate CS for types of applications such as high-speed imaging and high-dynamic range (HDR) imaging. Due to on-chip per-pixel exposure switching is not available on most image sensors, pixel-wise coded exposure is usually realized by discrete spatial-light modulators (SLMs) which make cameras suffer from bulky sizes and high power consumption. In this project, the designed CMOS image sensor is intended to implement on-sensor pixel-wise coded exposure. With a conventional camera packaging, CS applications are naturally extended to sensor nodes in a single frame period. In comparison to the state-of-the-art, the proposed on-sensor CS solution provides improved light throughput and in lower power consumption.



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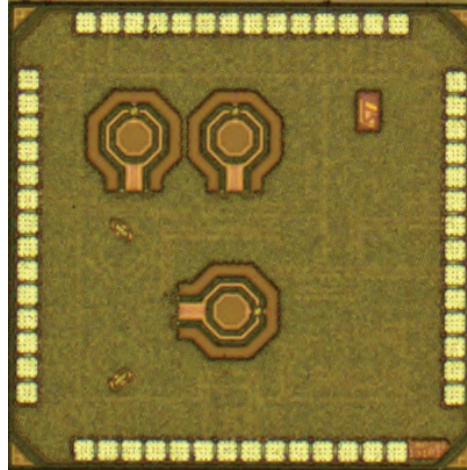
Kholdoun TORKI
Technical Director
Kholdoun.Torki@mycmp.fr



40Gb/s TIA and Optical Receiver
 Institution University of Alberta, Edmonton, Canada
<https://www.ualberta.ca>

CMP run ref.: 1802

Process Technology: ST 28nm CMOS28FDSOI

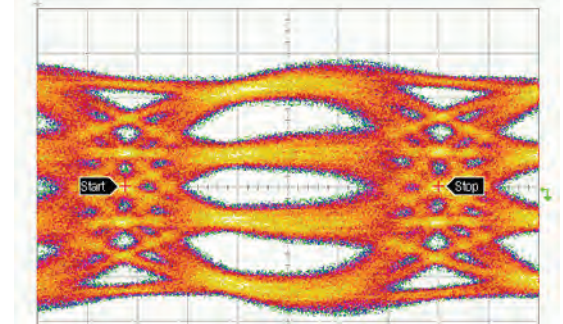


Circuit name: 1802CU_ICUAAMCP

Contact Name(s): Masum Hossain

E-mail(s): masum@uaberta.ca

Introduction / Application: The 40Gb/s optical receiver includes a TIA, discrete time equalizer and signal combiner.

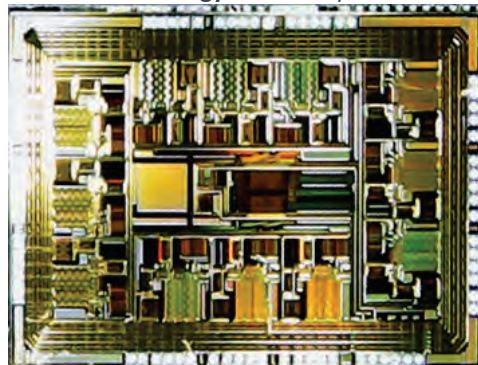


Description / Results: The TIA and front-end with discrete time signal processing allows 25 GHz BW targeting 40Gb/s performance. Gain-BW limitation of the CMOS process has limited achievable equalization limited. That is addressed in this work through discrete time integration. An example case is shown in the figure at 32 Gb/s.

Novel Integrated Solution for LED Signage
 University of Calgary, Calgary, Canada
<https://schulich.ucalgary.ca/contacts/majid-pahlevani>

CMP run ref.: 1801CV ICVCYL51

Process Technology: ams 0.35μm CMOS



Circuit name: Novel LED Driver

Contact Name(s): Majid Pahlevani

E-mail(s): majid.pahlevani@ucalgary.ca

Description / Results: The main objective of the research program is to provide an entirely new power architecture for future digital LED signage. The new architecture is based on an integrated solution distributed along the LED signage display. The integrated solution takes advantage of recent advances in high frequency power conversion and microelectronics in order to offer a highly efficient and compact solution for this application. This approach has several advantages such as: higher efficiency, compactness, less wiring, simpler heat removal, and no rotational component (fan-less). The novel architecture enables future digital LED signage displays to achieve optimal performance for each individual LED, leading to a highly efficient final product.

Introduction / Application: Currently, Light Emitting Diodes (LEDs) are dominating the lighting market because of their high energy efficiency and superior lifespan. One of the main applications of LEDs is in digital signage. Thus, the main focus of this project is on the design and implementation of an advanced integrated circuit for the digital LED signage industry.

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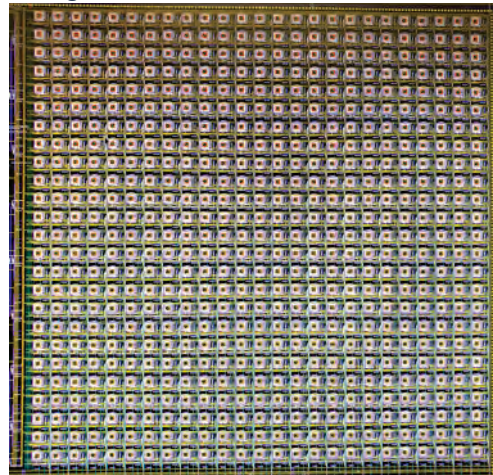
Kholdoun TORKI
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Kholdoun.Torki@mycmp.fr



Compact Time-Gated functional NIRS probe
Ecole Polytechnique de Montreal, QC, Canada
<https://www.polymtl.ca>

CMP run ref.: A35V18_4

Process Technology: ams 0.35 μ m CMOS-High Voltage H35B4D3

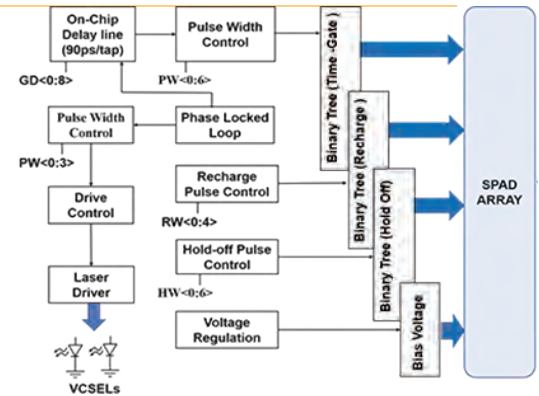


Circuit name: ICPMBMI

Contact Name(s): Frederic Lesage

E-mail(s): frederic.lesage@polymtl.ca

Introduction / Application: A novel integrated CMOS electronic and optical design was developed, incorporating gated detection and pulsed-laser illumination within a single chip, which will allow interrogating deeper tissue volumes with late time gates. Miniaturization is possible as the probes use detector and laser source places side-by-side, leading to a very small source-detector distance (SDD), which will allow interrogating deeper tissue volumes with late time gates. The compact size, flexibility, and customization possibilities can be considered as the first step towards portable multi-channel and multi-wavelength time domain near infrared spectroscopy (TD-NIRS) diagnostic tools for wearable healthcare applications.



Description / Results: We have proposed a novel system integrating a pair of two wavelength laser sources sensitive to oxygenated hemoglobin (HbO) and deoxygenated or reduced hemoglobin (HbR) and one time-gated 25 x 25 SPAD array detector. The detector gating technique for TCSPC allows probing at depth with small source-detector distance by rejecting the large signal from the surface which otherwise restricts the sensitivity of the probe to the vicinity of its tip. The size of each pixel is 24 μ m x 24 μ m with integrated fast readout interface electronics to achieve sub-nanosecond temporal resolution. The time-gate is synchronized with respect to the laser pulse by means of the on-chip delay line, whose output is propagated through balanced binary trees and serves as the control signal for the frontend of each SPAD pixel.

Publication references / link to web site:

S. Saha, Y. Lu, S. Weyers, M. Sawan, and F. Lesage, "Compact Fast Optode-based Probe for Single-Photon Counting Applications," IEEE Photonics Technology Letters, 2018.

S. Saha, Y. Lu, F. Lesage, and M. Sawan, "Wearable SiPM-based NIRS Interface Integrated with Pulsed Laser Source," accepted for publication in the IEEE Transactions on Biomedical Circuits and Systems (TBioCAS).

S. Saha, S. Burri, C. Bruschini, E. Charbon, F. Lesage, and M. Sawan, "Time Domain NIRS Optode based on Null/Small Source-Detector Distance for Wearable Applications," in 2019 IEEE Custom Integrated Circuits Conference (CICC), 2019: IEEE, pp. 1-8.

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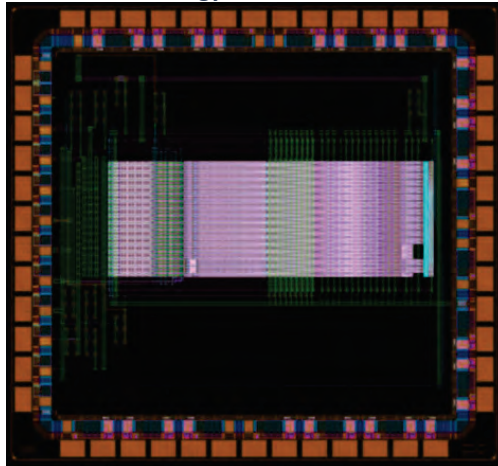
A low power 14 bits, 300KSps column ADC

XDIGIT, Grenoble, France

<https://www.xdigit.fr>

CMP run ref.: S13V18_1

Process Technology: ST130nm HCMOS9A

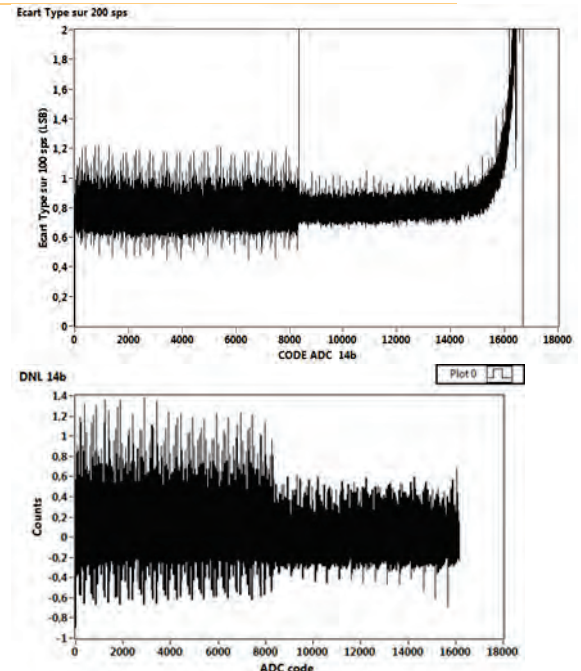


Circuit name: MASSAR

Contact Name(s): Daniel DZAHINI

E-mail(s): dzahini@xdigit.fr

Introduction / Application: MASSAR is a new converter's architecture suitable for high resolution column ADC for imaging applications. This design includes 32 columns featuring 14 bits of resolution. Each column needs only 24 μ m of pitch and dissipates 130 μ W while sampling at 300KHz.



Description / Results: Some testing results are shown here about noise (less than 1.2LSB rms), and differential non linearity issues (-0.6 to 1.3LSB so no missing code), which are the most critical parameters for our imaging applications.

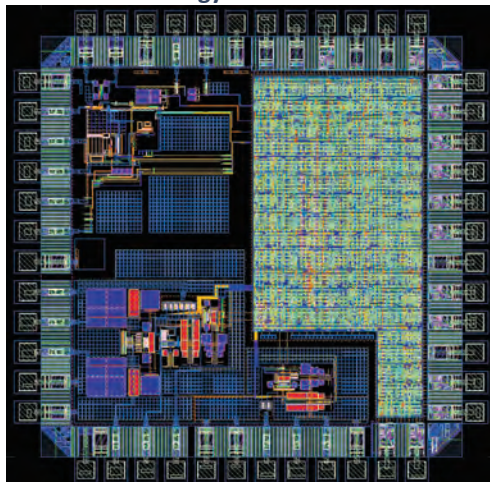
Wireless A/D interface for implant applications

Aalto University, School of Electrical Engineering, Espoo, Finland

<http://www.ele.aalto.fi>

CMP run ref.: S28I18_1

Process Technology: ST 28nm CMOS28FDSOI



Circuit name: EEGBIDE2_TOP

Contact Name(s): Olaitan Olabode

E-mail(s): olaitan.olabode@aalto.fi

Introduction / Application: The growing need for personalized healthcare is driving the development of low-power, compact and autonomous solutions for biomedical applications. In addition, the increasing speed of semiconductor processes as the technology node decreases, enables the development of more digital intensive solutions.

Description / Results: The implemented chip provides a wireless analog-to-digital (A/D) interface for implantable applications. The chip is realized as a mixed-signal design including a time-based analog-to-digital converter, digital signal processing unit, energy harvesting and communication modules

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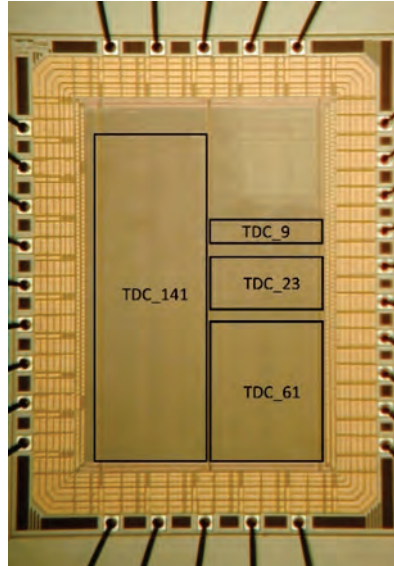
Kholdoun TORKI
Technical Director
Kholdoun.Torki@mycmp.fr



Time-to-Digital Converter based on a Self-Timed Ring Oscillator
 TIMA Lab - Grenoble INP, France / STRS Lab – INPT, Morocco
<http://tima.univ-grenoble-alpes.fr/tima/fr> / <http://www.inpt.ac.ma>

CMP run ref.: A35C18_3

Process Technology: ams 0.35 μ m C35B4C3



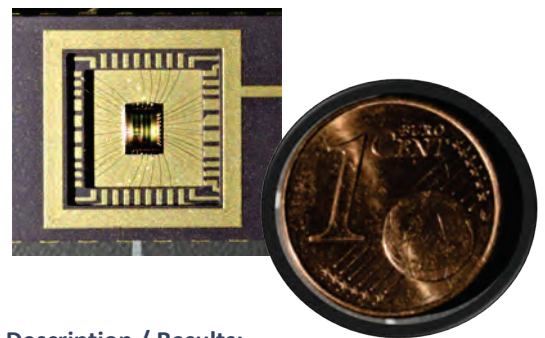
Circuit name: STRO-TDC

Contact Name(s): Laurent Fesquet

E-mail(s): Laurent.Fesquet@univ-grenoble-alpes.fr

Introduction / Application: Time-to-Digital Converters (TDCs) have become unavoidable in systems incorporating high precision time measurement. They are used in many application fields such as high-energy physics. We propose a new TDC architecture based on a Self-Timed Ring Oscillator (STRO), which is able to provide a very high resolution without averaging. Indeed, the proposed TDC virtually achieves a time resolution as fine as desired by

simply increasing the STRO number of stages. In fact, the STRO is a multi-phase oscillator, which is able to provide one phase per stage output. The TDC exploits these different STRO phases, which are evenly-spaced thanks to the unique analog STRO properties. Thus, a regular time base can be extracted from this STRO and applied for time measurement.



Description / Results:

4 TDCs with 9, 23, 61, and 141 stages have been integrated. The measurements are in accordance with our theoretical models. They prove the ability of the proposed TDC architecture to enhance the time resolution by increasing the number of stages. The measured time resolution of the smallest TDC is 72 ps, while a time resolution of 30 ps (resp. 14 ps) is obtained with the TDC of 23 (resp. 61) stages. This hardware implementation allows us to further evaluate the performance of the proposed TDC and confirm the advantages of the proposed approach. The fabricated circuit size is a 2.9mm x 2.2mm with a core area of 3.3 mm². A dual-in-line (DIL) ceramic package with 40 pads has been used for packaging the chip.

Publication references / link to web site:

A. El-Hadbi, A. Cherkaoui, O. Elissati, J. Simatic, and L. Fesquet, "An Accurate Time-to-Digital Converter based on a Self-Timed Ring Oscillator for On-the-fly Time Measurement". In Analog Integrated Circuits and Signal Processing, vol. 97, no. 3, pp. 471-481, Dec 2018. doi: 10.1007/s10470-018-1223-4

A. El-Hadbi, A. Cherkaoui, O. Elissati, J. Simatic, and L. Fesquet, "On-the-fly Sub-Gate Delay Resolution TDC based on Self-Timed Ring : A Proof of Concept". In 2017 15th IEEE International New Circuits and Systems Conference (NEWCAS'17), Strasbourg, France, 25-28 June 2017, pp. 305-308. doi : 10.1109/NEWCAS.2017.8010166

A. El-Hadbi, O. Elissati and L. Fesquet "Time-to-Digital Converters : A Literature Review and New Perspectives". In 2019 5th Conference on Event-Based Control, Communication and Signal Processing (EBCCSP'19), Vienna, Austria, May 27-29, 2019. doi :10.1109/EBCCSP.2019.8836857

Contacts:

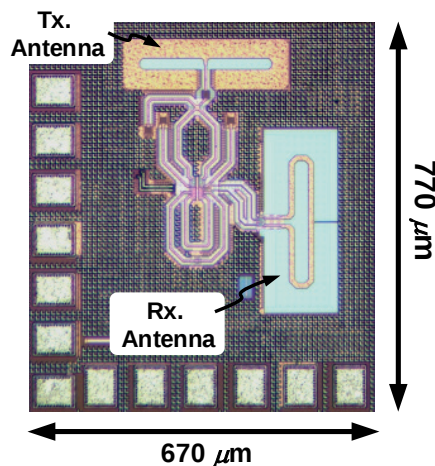
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A 220 GHz Ultra-Wideband FMCW Radar
University of Michigan, Ann Arbor, MI, USA
<http://unic.eecs.umich.edu>

CMP run ref.: S55S18_4
Process Technology: ST 55nm SiGe BiCMOS



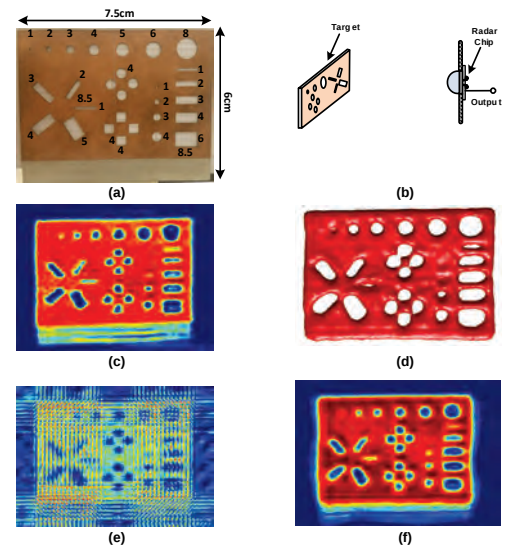
Circuit name: 220GHz Radar
Contact Name(s): Ehsan Afshari
E-mail(s): afshari@umich.edu

Introduction / Application: In this work, for the first time, a fully integrated imaging radar at THz/sub-THz frequencies is presented which demonstrate a fine lateral resolution without using any focal lenses/mirrors. We achieve a lateral resolution of 2mm for an object at 23cm distance as well as a range resolution of 2.7 mm.

Publication references / link to web site:

A. Mostajeran, M. Naghavi, M. Emadi, S. Samala, B. Gingsburg, M. Aseeri, and E. Afshari, "A High Resolution 220GHz Ultra-Wideband Fully Integrated FMCW ISAR Imaging System" IEEE Transactions on Microwave Theory and Techniques, Jan. 2019.

A. Mostajeran, H. Aghasi, H. Naghavi, and E. Afshari, "Fully Integrated Solutions for High Resolution Terahertz Imaging," Proc. of IEEE Custom Integrated Circuits Conference (CICC), 2019 (Best invited paper award).



Description / Results: To obtain the fine lateral resolution, we use near-field beam-forming algorithm based on the ISAR systems. The synthesized beamwidth is less than 0.5 degree. To achieve the decent range resolution, in a FMCW radar configuration, a state-of-the-art chirp bandwidth of 62.4GHz at a center frequency of 221.1GHz is generated and efficiently radiated. The level of integration and the bandwidth is the best among all published works.

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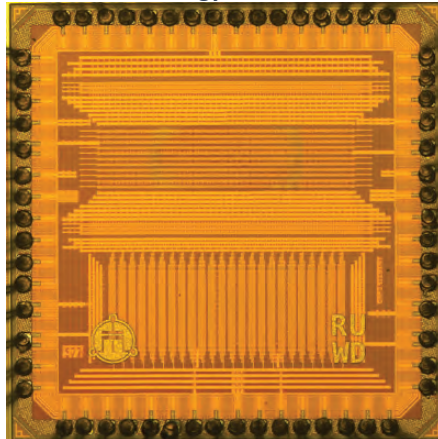
Kholdoun TORKI
Technical Director
Kholdoun.Torki@mycmp.fr



A near/sub-threshold RISC-V micro-processor!
 MICAS - ESAT - KULEUVEN, Leuven, Belgium
<https://www.esat.kuleuven.be/micas/>

CMP run ref.: S28I19_1

Process Technology: ST 28nm CMOS28FDSOI



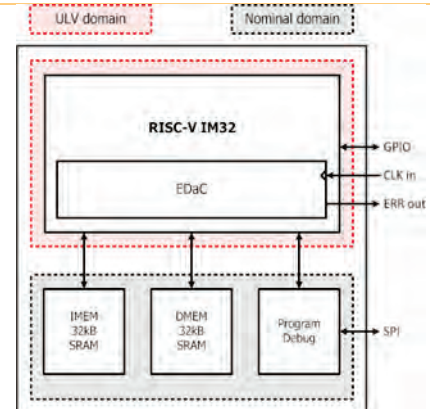
Circuit name: PSCALE_C

Contact Name(s): Roel Uytterhoeven, Wim Dehaene

E-mail(s):

roel.uytterhoeven@esat.kuleuven.be,
 wim.dehaene@esat.kuleuven.be

Introduction / Application: The PSCALE chip is a small RISC-V micro-processor using the RISC-V IM32 ISA. It targets a versatile range of energy constraint applications where low to medium processing speeds are desired e.g. medical implants, IoT sensor nodes,...

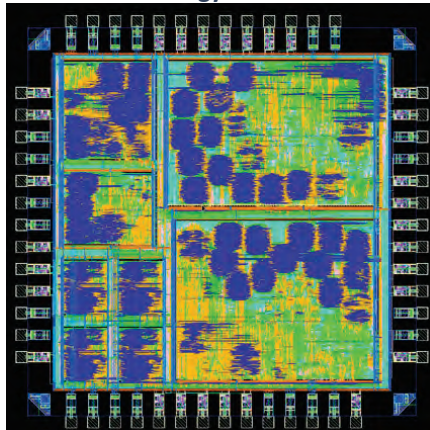


Description / Results: To maximize energy efficiency, the RISC-V processor is implemented at near/sub-threshold supply voltage. This enables operation in the minimum energy point (MEP) of the device. FDSOI's unique body-biasing capabilities allow to tune the MEP towards any desired operation point. Further, the processor is equipped with a Timing-Error Detection and Correction (EDaC) technique to overcome the large design margins typically encountered at near/sub-threshold supply voltages. Thanks to the EDaC, the device is able to operate at first point of failure with minimal voltage margin.

Hardened GPS trackers
 IMT Atlantique, Brest, Brittany, France
<https://www.imt-atlantique.fr/fr>

CMP run ref.: S28I19_1

Process Technology: ST 28nm CMOS28FDSOI



Circuit name: Cyril Lahuéc Tracker_GPS

Contact Name(s): Cyril Lahuéc

E-mail(s): cyril.lahuéc@imt-atlantique.fr

Introduction / Application: Transistor shrinking dimensions and reduced supply voltages to save energy cause faulty logic gates. Several hardening techniques have been proposed and studied during the Cominlabs project RELIASIC (REliable ASIC). The integrated circuit implemented uses these techniques to hardened several version of a GPS tracker and a standard one for comparison purpose. The FDSOI technology allows modifying locally the substrate biasing to induce logic gate errors as the supply voltage decreases to few hundreds of millivolts. The implemented techniques efficiency will be assessed also with temperature variations and faults injected by LASER pulses

Description / Results: the circuit is currently being tested

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Thales

<https://www.thalesgroup.com>

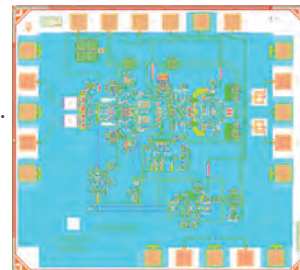
Description / Results: Circuits are currently being tested.

CMP runs ref.: S13S18_1, S13S18_2 and SS13S18_1

Process Technology: ST 130nm SiGe BiCMOS

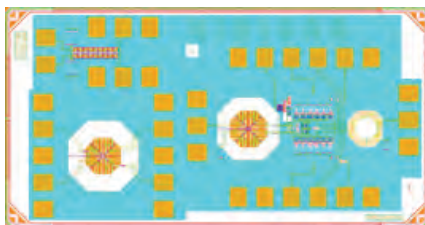
Contact Name(s): Vincent PETIT

E-mail(s): vincent-f.petit@fr.thalesgroup.com



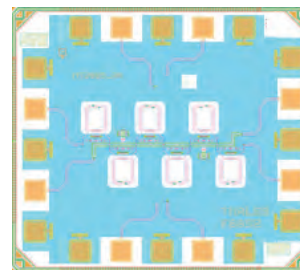
Circuit name: CMP13S181T0, MT18B9_AA

Test Structures: Wide Bande Sample & Hold



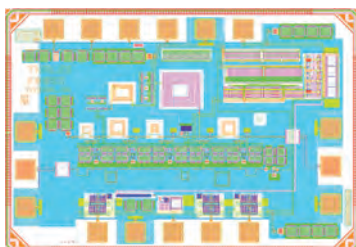
Circuit name: CMP13S181T2, HIBIS_AA

Test Structures: Limiter / Coupler



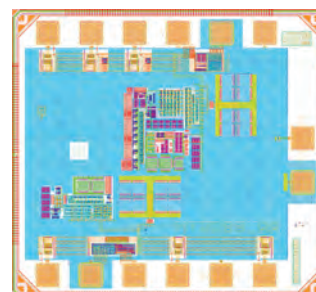
Circuit name: CMP13S181T3, MT20B9_AA

Test Structures: True delay line



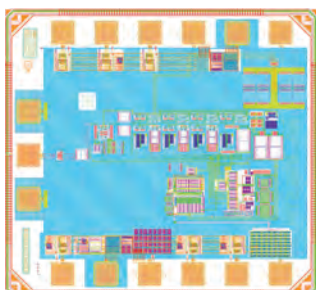
Circuit name: CMP13S182U3, MT21B9_AA

Test Structures: RF Attenuator



Circuit name: CMPS13S181A3, MT22B9_AA

Test Structures: Thermal sensor

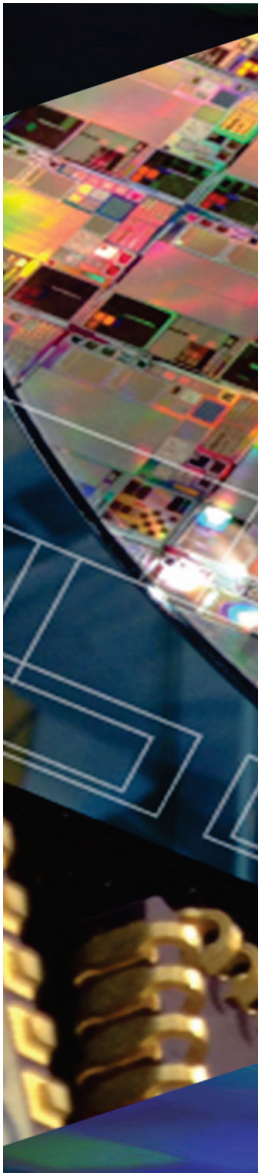


Circuit name: CMPS13S181A4, MT23B9_AA

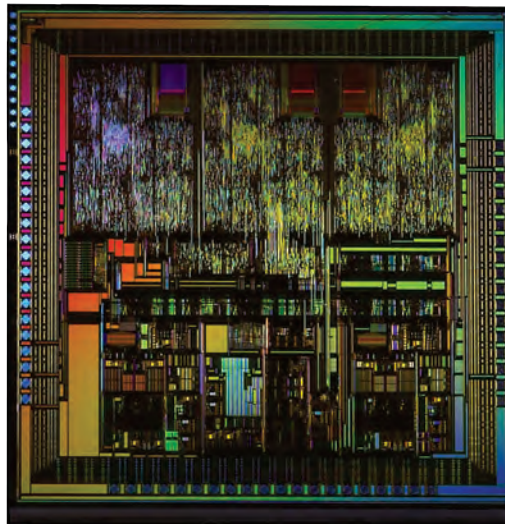
Test Structures: Level detector

Circuit name: CMPS13S181A9, JUPITER_AA

Test Structures: Power Amplifier



Please turn the booklet upside down for the process catalog 2020.



Courtesy of IM2NP

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