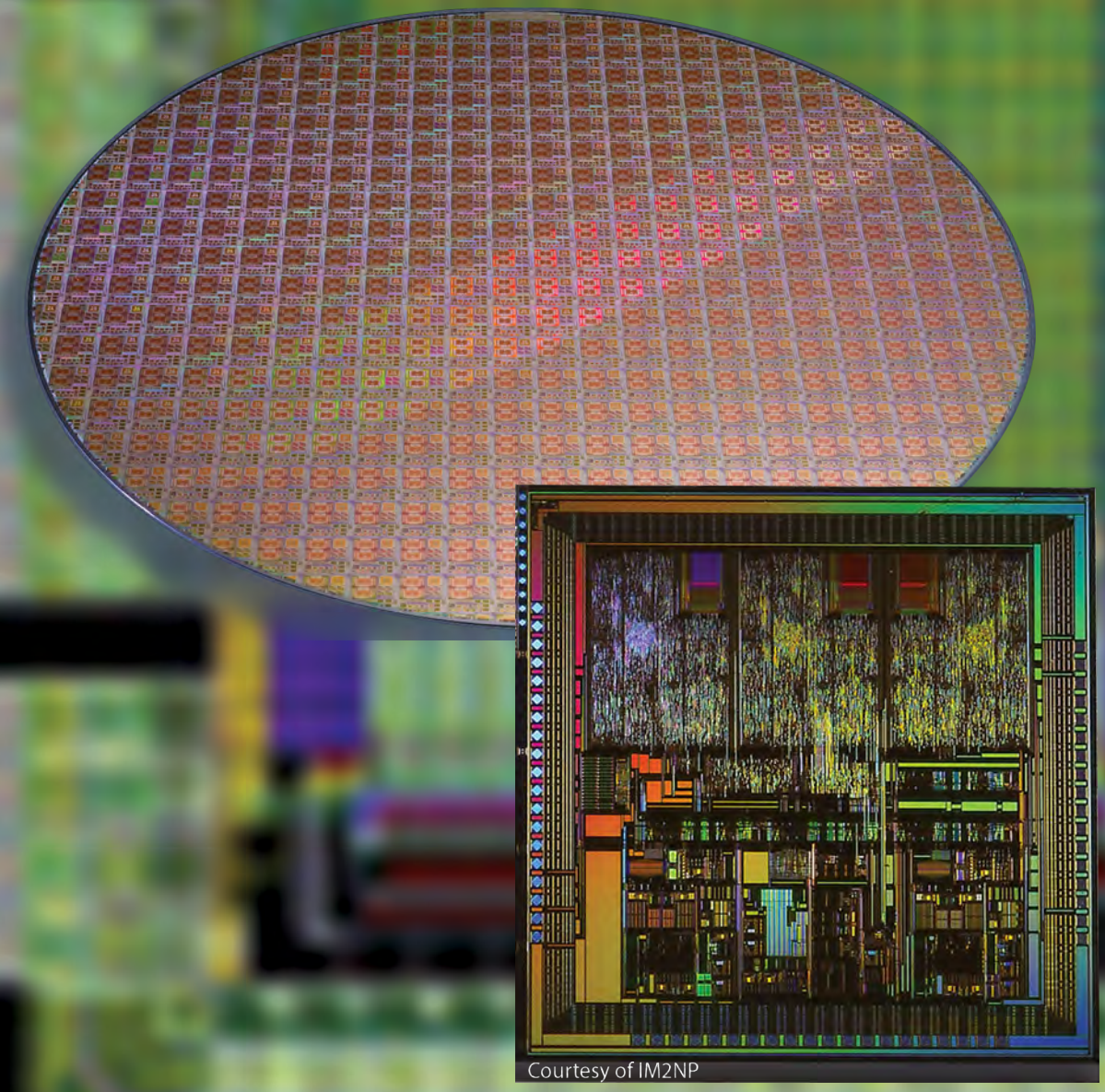
Multi-Project Wafer (MPW) Service Center

Circuits Multi-Projets®

From layout to chips

Process catalog 2020



Courtesy of IM2NP

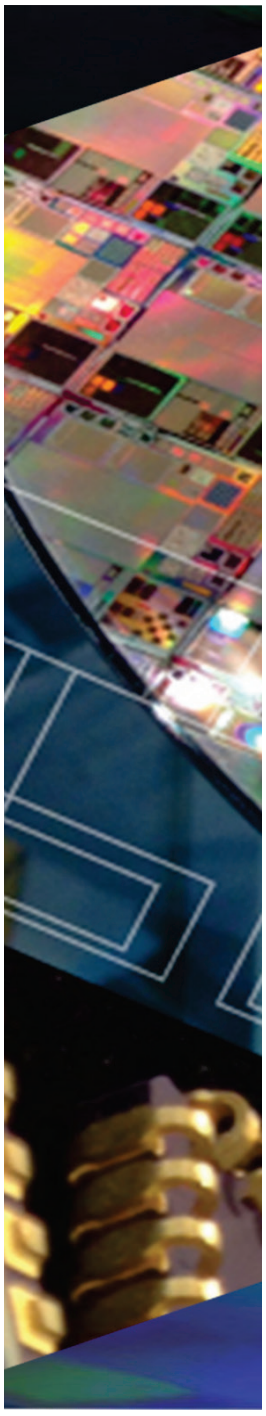
https://mycmp.fr

CMP
46, Avenue Félix Viallet
38000 Grenoble - France
Ph.: +33 4 76 57 46 17
Fax: +33 4 76 47 38 14
E-mail: cmp@mycmp.fr

cnrs Grenoble INP UNIVERSITÉ Grenoble Alpes

EUROPRACTICE European Commission Horizon 2020 European Union funding for Research & Innovation

Table of contents



Editorial

Dear CMP users,

F For the coming year, CMP is engaged with its suppliers, providers and partners to straighten the process portfolio. 2019 has seen the introduction of new technologies and new providers. For 2020 the objective is to expand the technology portfolio and improve the quality service.

In this process catalog, you will find more about the new services, with ONsemi, em microelectronics, AMF through CMC and very recently SMIC among others. CMP is pleased to introduce new services with new providers answering the community needs. Regarding ams technologies, in 2020 CMP and Fraunhofer are joining efforts in order to serve institutions that still needs to access the ams portfolio. Although CMP has engaged partnerships with several suppliers regarding “mature” CMOS technologies, CMP is committed to help the long terms users on ams technologies, and help them completing their research activities build over many years with ams.

2020 should also provide a visible move regarding CMP services on STMicrotechnologies. After 2018 and 2019 years with difficulties to operate reliable MPW services on the most advanced technologies, a strong partnership, within the frame of IPCEI Nano2022, is expected to raise the quality of services. The objective is to operate reliable MPW shuttle runs and increase the support on advanced technologies: more tutorials, trainings, additional IPs, …

2020 will bring new services with new partners or new technologies. By the time this Edito is written, it is too early to state on them. Some news will come up during this coming year. We are very happy to see that, after several years of prospections, CMP is stepping forward, in several fields. Regarding Photonics and related topics, we are now aggregating a very complementary portfolio straightening CMP team to address these technologies. We will be also targeting to offer new smart power and printed electronics services for the benefits of new communities of users. This diversification is important for CMP and users, to prepare next generation of services.

In 2020 CMP will operate its services, entirely on myCMP webapp, fully developed and implemented. We will have some improvements to implement. This web app will bring satisfactions from the Users’ community. The constructive feedbacks from CMP users are of a great help for improving this interface. We sincerely apologize for any unpleasantness that occurred while setting up this interface.

Year 2020 have the event of change of the CMP Director. Kholdoun Torki will have this role, ensuring together with the CMP team the continuation of the CMP service.

CMP is committed continuing to serve the community for the best: MPW services, low volume productions, and partnership with providers. This second year within Europractice will also show up the contribution of CMP to the community of both academia and R&D industry.

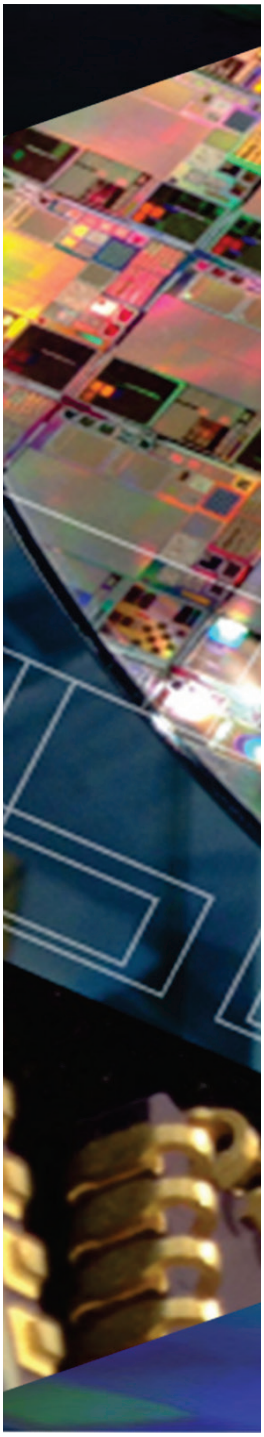
We wish you all a pleasant working experience with CMP.

Koldoun Torki, Jean-Christophe Crébier

Circuits Multi-Projets®
(CMP)
Multi-Project Circuits®

From Layout to Chips

mycmp.fr



From Layout to Chips

Check for new prices
mycmp.fr

Process catalog

ICs, Photonics & MEMS prototyping & low volume production

Circuits Multi-Projets® (CMP) is a Multi-Project Wafer (MPW) service organization in Integrated Circuits (ICs), Photonic ICs and Micro Electro Mechanical Systems (MEMS) for prototyping and low volume production. Circuits are fabricated using industrial process lines for universities, research laboratories and industrial companies. Since 1981, 645 customers from 71 countries have been served, more than 8307 projects have been prototyped through 1142 MPW runs and 74 different technologies have been interfaced.

CMP distributes Process Design kits (PDK) for CMOS/BiCMOS IC's, Photonic IC's and MEMS' technologies . Each of them contains technology files, simulation models, design rules, standard cell libraries. A copy of any requested design kit can be sent to customer after a non-disclosure agreement (NDA) with CMP. Customer request and support are provided through myCMP: https://crm.mycmp.fr

CMOS/BiCMOS/SiGe/OxRAM NVM Integrated Circuits by feature size order.

STMicroelectronics	28nm	FDSOI	CMOS28FDSOI
STMicroelectronics	55nm	SiGe	BiCMOS055
STMicroelectronics	65nm	CMOS	CMOS065
STMicroelectronics	130nm	SiGe	BiCMOS9MW
STMicroelectronics	130nm	SOI	H9SOI-FEM
STMicroelectronics	130nm	CMOS	HCMOS9A
IRT Nanoelec/LETI-CEA	130nm	CMOS	MAD200
STMicroelectronics	0.16µm	BCD	BCD8sP
STMicroelectronics	0.16µm	BCD-SOI	BCD8s-SOI
em microelectronic	0.18µm	CMOS	EMALPC18 logic
ON Semiconductor	0.18µm	CMOS	ONC18MS
ON Semiconductor	0.18µm	HV-CMOS	ONC18I4T
ON Semiconductor	0.35µm	CMOS	ONC35U
ON Semiconductor	0.35µm	HV-CMOS	ONC35I3T25U
ON Semiconductor	0.35µm	HV-CMOS	ONC35I3T50U
ams	0.35µm	CMOS	C35B4C3
ams	0.35µm	CMOS Opto ARC	C35B4O1
ams	0.35µm	CMOS Opto BARC	C35B4OA
ams	0.35µm	SiGe BiCMOS	S35D4M3
ams	0.35µm	HV-CMOS	H35B4D3
ams	0.35µm	SiGe BiCMOS	S35D4M5 DLP/4LM

Silicon Photonic Integrated Circuits

IRT Nanoelec/LETI-CEA	Si-Photonics	Si310–PHMP2M
AMF	Si-Photonics	fabrication process AMF

MEMS - Micro Electro Mechanical Systems

ams	0.35µm	CMOS Bulk Micromachining: front-side & back-side
MEMSCAP	MEMS	PolyMUMPs
MEMSCAP	MEMS	SOIMUMPS
MEMSCAP	MEMS	PiezoMUMPs

Packaging for Prototyping & Low Volume Production

CMP offers a wide variety of standard packages and assembly services for prototyping and low volume production. **Before starting a design**, an important step is to **select a package** and/or a packaging technique. Die package compatibility optimization can significantly impact the overall system performances.

Contacts:

Christelle RABACHE
Technical Manager
Christelle.Rabache@mycmp.fr

Alejandro CHAGOYA
Senior IT Manager & DK Support
Alexandre.Chagoya@mycmp.fr

Yann YEBE
Design-Kit Support Engineer
Yann.Yebe@mycmp.fr

Kit support contact:
cmp-support@mycmp.fr

Design kits (DK) and support

CAD tools supported

Tables below present EDA tools and design flows available with the materials and design kits distributed by CMP from our foundry partners. Do not hesitate to check our website for latest design kits releases and supported EDA tools to set up your design environment, prior to design and submit a project. When a new version of a design kit is published, all institutions whose NDA/CLA is valid, are eligible to automatically receive the update.

STMicroelectronics design kits

	Analog / Mixed flow			Digital flow*				Verifications
	Schematic & Layout	Electrical Simulation	PEX	Logic Synthesis	Digital Simulation	Place & Route	Final Analysis	LVS & DRC
Cadence	IC 6.1.6 / 6.1.7	Spectre	QRC	Genus	Xcelium	Innovus	Tempus Voltus	PVS*
Mentor Graphics	-	Eldo	-	-	-	-	-	Calibre
Synopsys	-	Hspice*	StarRCXT*	Design Compiler	-	-	PrimeTime Formality	-
Keysight	-	Goldengate*	-	-	-	-	-	-

* CAD tools supported only for some ST's technologies

em microelectronic design kit

	Analog / Mixed flow			Digital flow				Verifications
	Schematic & Layout	Electrical Simulation	PEX	Logic Synthesis	Digital Simulation	Place & Route	Final Analysis	LVS & DRC
Cadence	IC 6.1.7	Spectre	QRC	RTL Compiler	Incisive	Encounter	-	PVS

ON Semiconductor design kits

	Analog / Mixed flow			Digital flow				Verifications
	Schematic & Layout	Electrical Simulation	PEX	Logic Synthesis	Digital Simulation	Place & Route	Final Analysis	LVS & DRC
Cadence	IC 6.1.6 / 6.1.7	Spectre	-	RTL Compiler	Incisive	Encounter	Conformal	-
Mentor Graphics	-	-	Calibre	-	-	-	-	Calibre
Synopsys	-	-	-	Design Compiler	-	-	PrimeTime Formality	-

ams HitKit v4.10 ISR15

	Analog / Mixed flow			Digital flow				Verifications
	Schematic & Layout	Electrical Simulation	PEX	Logic Synthesis	Digital Simulation	Place & Route	Static Timing Analysis	LVS & DRC
Cadence	IC 6.1.6	Spectre UltraSim	QRC	RTL Compiler	Incisive AMS-Designer	Encounter	-	Assura
Mentor Graphics	-	-	-	-	QuestaSim	-	-	Calibre
Synopsys	-	Hspice	-	Design Compiler	-	-	PrimeTime	-

Design kits (DK) and support

Contacts:

Christelle RABACHE
Technical Manager
Christelle.Rabache@mycmp.fr

Alejandro CHAGOYA
Senior IT Manager & DK Support
Alexandre.Chagoya@mycmp.fr

Yann YEBE
Design-Kit Support Engineer
Yann.Yebe@mycmp.fr

Kit support contact:
cmp-support@mycmp.fr

Silicon photonic design kits

	Schematic & Layout	Simulation	DRC Verification
NANOELEC leti	Cadence IC 6.1.7 Synopsys OptoDesigner Tanner	Mentor Graphics Eldo	Mentor Graphics Calibre
amf ADVANCED MICRO FOUNDRY	Luceda-Tanner	Luceda CAPHE	Mentor Graphics Calibre

MEMS design kits

	Technology	Software	DRC Verification
amf	Bulk Micromachining	Cadence IC 6.1.6	Cadence Assura Mentor Graphics Calibre
MEMSCAP The Power of a Small World™	PiezoMUMPS PolyMUMPS SOIMUMPS	Cadence IC 6.1.6	Cadence Assura

Technical support on the design-kits

CMP provides technical support on the design-kits. Support at several levels is addressed: DK retrieval and installation issues, difficulties in the use of the design platforms or the CAD tools, questions about the design-flow, etc.

Starting 2020, access to the technical support is fully integrated into the new myCMP custom-relation portal. The technology manager of each institution autonomously creates an account for the designers, so that they can take advantage of all the services offered on myCMP.

mycmp **https://crm.mycmp.fr**

The support interface is based on a ticketing system. Design kit users open a new ticket for each technical question. CMP staff member in charge of the ticket posts information about the ongoing investigation of the subject.
Different actions can be envisaged in order to find a solution:

- a careful check of the design kit documentation and of CMP knowledge data base
- the elaboration or the request-to-the user of a test case reproducing the issue
- and, when nothing of the above is enough to answer the question, submission to the support structure of the design kit provider.

Once the solution is known, it is sent on the corresponding ticket. Several exchanges between CMP staff and the user may eventually be required depending on the complexity of the problem.

This help desk has been set-up to offer designers a higher level of service quality on the follow-up of their support requests. Design kit users can easily open new tickets, check the progress status of those already open and even consult those who have been solved. Each time a new message is posted by CMP staff, a notification is sent by e-mail to the concerned users.
All the data exchanged for a given problem such as tool versions, screen snapshots, test cases, log files, etc. are available inside the same ticket thread, so that the relevant information can be quickly accessed both by CMP staff and by the user.

All the DK support services will be carried carried out through this new web interface.

Design kits (DK) and support

Tutorials and DK documentation

Several documents, data-sheets and user's guides exist inside the design platforms under "doc" folders. The Design Rule Manual (DRM) is delivered separately from the design kit for confidentiality reasons. Once a NDA/CLA is signed, the institution receives the necessary information to access this documentation.

Different tutorials have also been developed by CMP support team addressing a large variety of topics such as Monte-Carlo simulation, LVS bbox methodology, parasitic extraction flows, etc. A list of available tutorials can be found on myCMP. They are technology-dependent and design-kit-version dependent, and can be obtained upon request. Tutorials are only available for institutions with a valid NDA/CLA.

All these materials are useful for starting using the design-kits, showing the different design-flow steps, the correct use of tech-files and libraries, and the rules to observe for high quality circuit(s).

IPs offer

Intellectual Properties (IPs) are complete blocs that can be used "as is" in an integrated circuit. Either designed by the DK provider, or by final end users, they always integrate a very specific functionality like retention cells, level shifters, PLL, etc.

Today, some IPs can be accessed from the DK provider. Especially, memory blocs as RAM and ROM can be generated for most of the offered technologies. Designers can request these IPs through their myCMP web account.

https://crm.mycmp.fr

Designers can also enjoy specific IPs available thanks to our industrial or academic partners. A list of this kind of service is accessible on our web site: https://mycmp.fr/services/add-on-services/

CMP staff is working on the elaboration of a new platform, to make basic IPs developed by CMP community, available to other institutions who are working on the same technology.
This platform will offer several opportunities:

- if you previously developed a design: you can share valuable elements of your work to help future designers ➔ the benefit for you: your department/institution is **mentioned in every publications of circuits using your IP(s)!**
- if you are starting a new design: you can access a database of ready to use IPs, which can be directly integrated into your circuit ➔ the benefit for you: this is **fully free of charge!**

The IP sharing will be possible with a legal framework, for both parties: IP provider / IP user. CMP will act as an intermediary for the delivery of these IPs: all the data are saved on a secured CMP server and will be provided, on request, to institutions who signed a dedicated license contract.

If you are interested to share some of your blocks, don't hesitate to contact us!

Moreover, CMP carried out a user's survey to take note of the needs of its community in terms of IPs. Different developments already started to design some IPs compatible with ST's CMOS28FDSOI advanced node. Other offers are also ongoing to provide IPs for more mature technologies.

IPs portfolio available through CMP IP portfolio and IP sharing services through CMP will be made available in 2020.

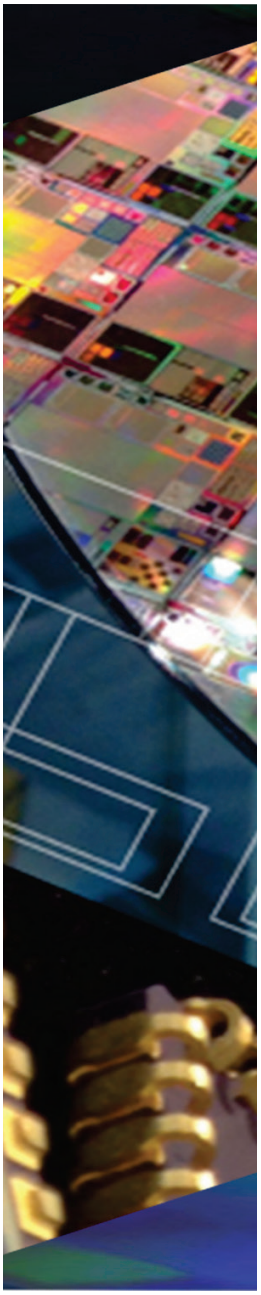
Contacts:

Christelle RABACHE
Technical Manager
Christelle.Rabache@mycmp.fr

Alejandro CHAGOYA
Senior IT Manager & DK Support
Alexandre.Chagoya@mycmp.fr

Yann YEBE
Design-Kit Support Engineer
Yann.Yebe@mycmp.fr

Kit support contact:
cmp-support@mycmp.fr



Contact:

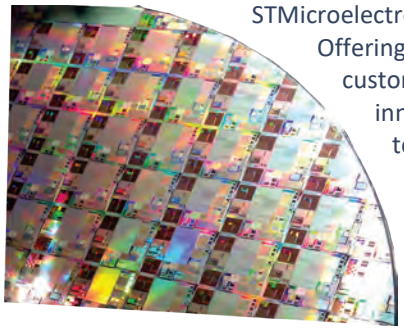
Jean-François PAILLOTIN
Lead Manager MPW Run/ STMicroelectronics
Jean-Francois.Paillotin@mycmp.fr

DK support contact:
cmp-support@mycmp.fr

Technology overview

Integrated circuits

STMicroelectronics

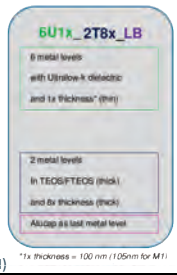
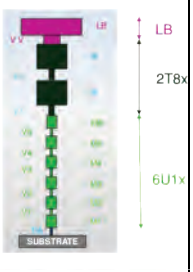


STMicroelectronics is one of the world's largest semiconductor companies. Offering one of the industry's broadest product portfolios, ST serves customers across the spectrum of electronics applications with innovative semiconductor solutions by leveraging its vast array of technologies, design expertise and combination of intellectual property portfolio, strategic partnerships and manufacturing strength. CMP has been offering STMicroelectronics technologies since 1992.

28nm CMOS FD-SOI 8ML

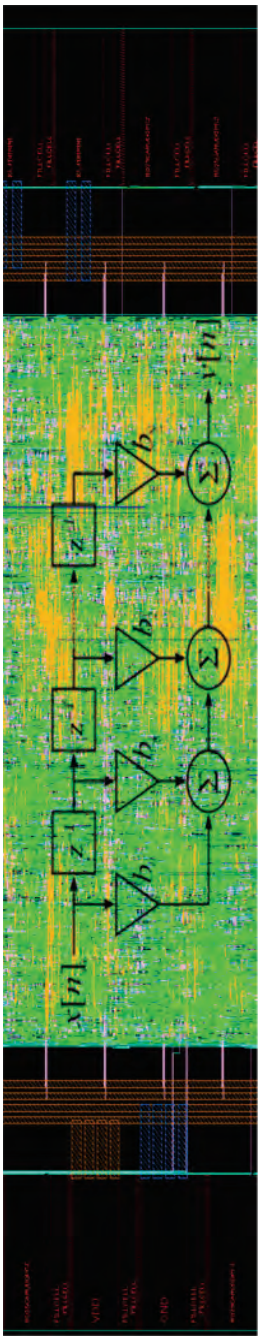
Several process steps and masking levels are removed from the 28nm bulk process. This compensates the extra cost of the SOI substrate wafers. FD-SOI has lower channel leakage current. Carriers are efficiently confined from source to drain: the buried oxide prevent these carriers to spread into bulk. The process comes with NMOS and PMOS devices including body-bias-voltage scaling from 0V to +2V that helps decreases minimum circuit operating voltage. Standard-cells libraries are characterized over a range of voltages from 300mV to 1.2V.

Transistors can be ideally controlled through independent bias voltages. These body bias techniques allow dynamically modulating the transistor threshold voltage. Dynamic voltage and frequency scaling (DVFS) techniques can be applied more efficiently than alternative processes, therefore achieving high performance at conventional voltages.The 28nm fully depleted silicon on insulator process from STMicroelectronics has the following features:

TECHNOLOGY: CMOS28FDSOI	**STMicroelectronics IC 28nm CMOS28FDSOI Advanced CMOS FDSOI**
Process characteristics	CMOS gate length: 28nm drawn poly length Triple well Fully Depleted SOI devices, with ultrathin BOX and Ground Plane Body biasing Dual Vt MOS transistors (LVT, RVT) Dual gate oxide (1.0V for core and 1.8V for IO) Temperature range: -40°C to 175°C Dual-damascene copper for interconnect, low-k dielectric 8 metal layers (8ML) for interconnect 2 thick Cu top metal (0.880 micron) Low k inter-level dielectric Fringe MoM capacitors Inductors Analog / RF capabilities Various power supplies supported: 1.8V, 1.0V Standard cell libraries (more than 3Mgates/mm2) Embedded memory (Single port RAM / ROM / Dual Port RAM)  
Application area	Internet of Things, Wearable Ultra-low-voltage operation FBB optimizes power/performance Efficient RF and analog integration Automotive Well-managed leakage in high-temperature environments High reliability thanks to highly-efficient memories Networking Infrastructure Energy-efficient multicore Adapt performance & power to workload via FBB Excellent performance in memories Consumer Multimedia Optimized SoC integration (Mixed-signal & RF) Energy-efficient SoC under all thermal conditions Optimized leakage in idle mode
Design kits version	1.2 (Sept.-19)
DK front-end/back-end tools	Cadence IC 6.1.7
Price & Fabrication schedule	***Check mycmp.fr for new prices***
Packaging	*All packages provided by CMP*

More information: An Introduction to FDSOI: **https://mycmp.fr/datasheet/ic-28nm-cmos28fdsoi**

Technology overview



Contacts:

Christelle RABACHE
Technical Manager
Christelle.Rabache@mycmp.fr

Alejandro CHAGOYA
Senior IT Manager & DK Support
Alexandre.Chagoya@mycmp.fr

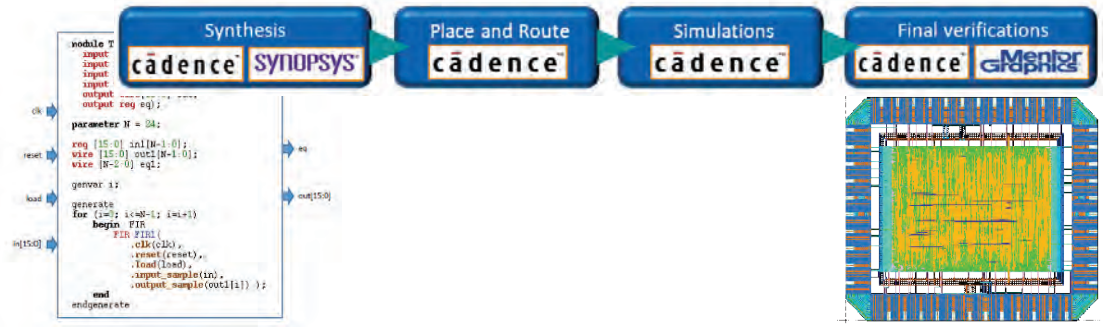
Yann YEBE
Design-Kit Support Engineer
Yann.Yebe@mycmp.fr

DK support contact:
cmp-support@mycmp.fr

28nm CMOS FD-SOI RTL to GDS design flow tutorial

Within the frame of the technical support, CMP has developed a complete tutorial to introduce the design methodology of a digital circuit in CMOS28FDSOI technology. As a walkthrough user guide, it details all the basic steps of a standard digital flow: ***from the RTL netlist to the GDS layout***. All corresponding scripts and testbenches files are provided in the tutorial package. The designers can thus, execute the suggested design flow. It can be easily adapted to other projects.

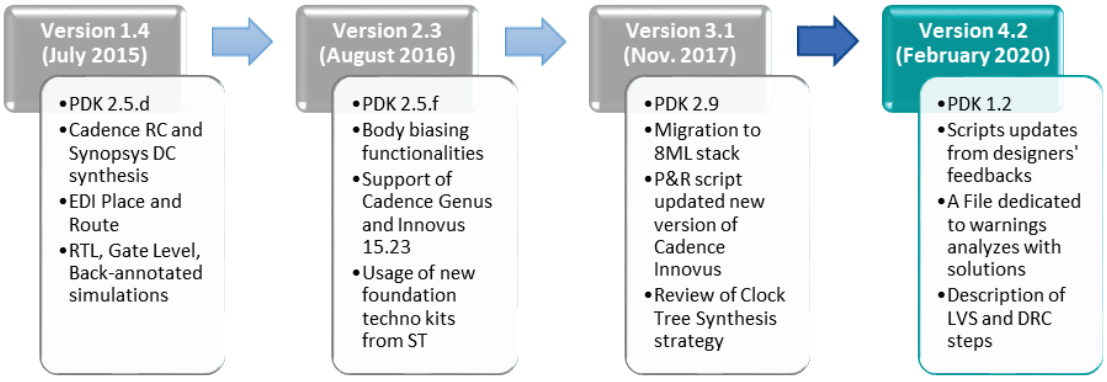
This tutorial illustrates, as an example, the design of a basic synchronous and sequential circuit: a Finite Impulse Response (FIR) filter. The digital implementation flow for this 28nm FDSOI technology is based on different CAD vendors' tools: Cadence, Mentor Graphics and Synopsys. One can perform synthesis, place and route, simulations and finally launch DRC and LVS verifications.



Digital design flow and CAD tools supported

The whole tutorial is regularly upgraded, keeping in mind the ***particularities of this 28FDSOI advanced node***, and integrating specific functionalities like body biasing. The main document, the scripts and the testbenches are regularly updated to remain compatible with latest PDK version and digital design tools releases.

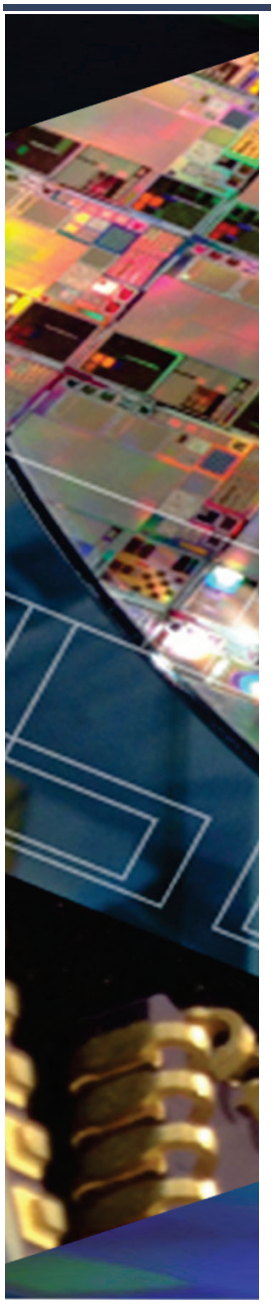
CMP support team is currently finalizing an update of this RTL to GDS tutorial, ***based on latest PDK release 1.2***. The delivery is planned for beginning of 2020. It will detail LVS and DRC final steps, with in addition the analysis of the different warning messages the designer may encounter during P&R process.



Versioning of CMP's digital design flow tutorial

This new distribution will be delivered to every institution with NDA/CLA in place for CMOS28FDSOI advanced node. If you need further information or any help using this tutorial, do not hesitate to contact us!

Technology overview



55nm BiCMOS SiGe 8ML

The BiCMOS055 technology of STMicroelectronics is well adapted for applications that are needing RF performance for analog part and high performance in digital part.

Bipolar SiGe transistors offer gain and high speed performances for analog devices:

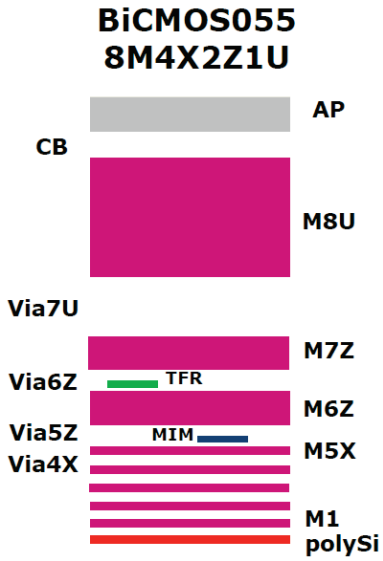
- F_t = 320GHz, f_{max} = 370GHz

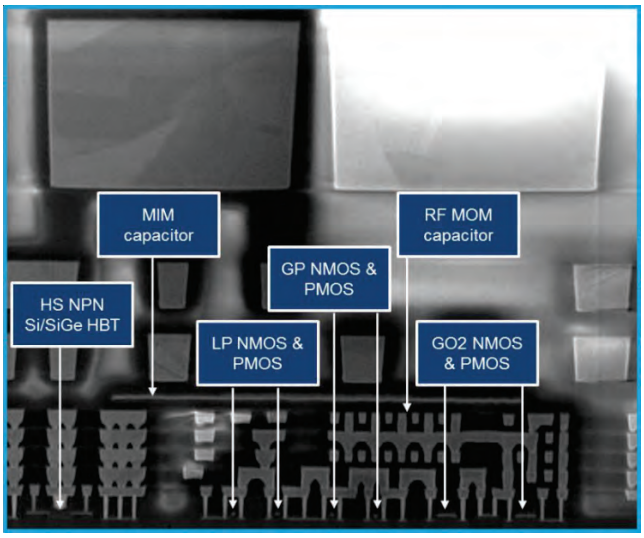
CMOS 55nm transistors enable high speed and high density for digital devices:

- 700 kgates/mm² for high speed gates
- 970 kgates/mm² for high density gates

Examples of analog/RF applications:

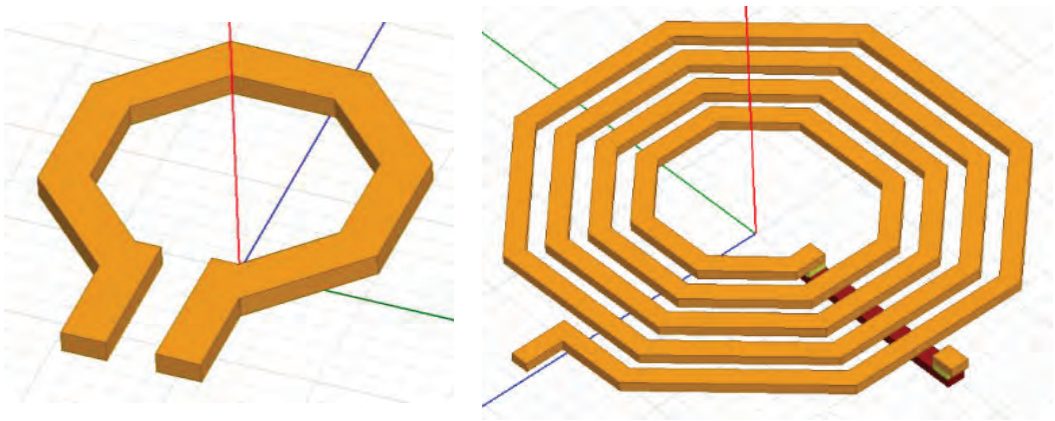
Automotive radar (24/77GHz)	LAN RF transceivers (60GHz)
Point-to-point radio (V-Band/E-Band)	Transmitters in THz frequencies
Vector modulators (60GHz)	





Cross section (courtesy of STMicroelectronics)

The process offers 8 copper layers for connections and an aluminum capping layer on pads. The 5 thin layers (M1 to M5X) are dedicated to high density connections, the 2 medium-thickness layers (M6Z and M7Z) are dedicated to supply and the thick layer is dedicated to RF signals.



3D views inductors (courtesy of STMicroelectronics)

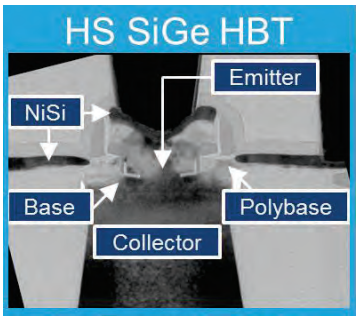
Contact:

Jean-François PAILLOTIN
Lead Manager MPW Run/
STMicroelectronics
Jean-Francois.Paillotin@mycmp.fr

DK support contact:
cmp-support@mycmp.fr

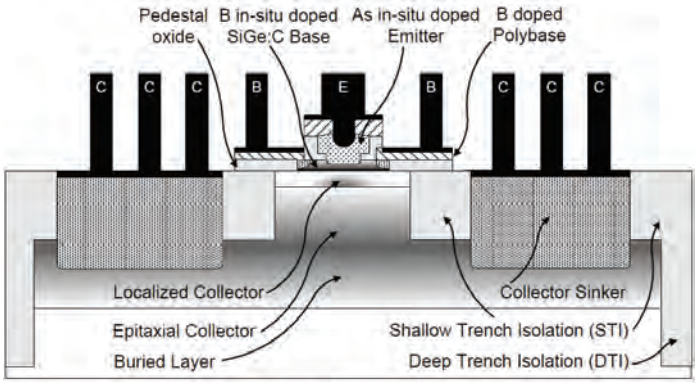
Technology overview

The thick metal 8 layer is well adapted for inductors and for transmission lines. Analog applications are improved by high-precision MIM capacitors, thin film resistors (TFR, should be available for CMP runs in 2016) and SiGe bipolar transistors.



High speed SiGe HBT transistor (courtesy of STMicroelectronics)

TECHNOLOGY: BiCMOS055	STMicroelectronics IC 55nm BiCMOS055 BiCMOS SiGe
Process characteristics	CMOS Gate length: 55nm drawn poly length Deep Nwell and Deep Trench Isolation Triple Vt MOS transistors (LVT, RVT and SVT) Low Power and General Purpose MOS transistors Dual gate oxide (1.0V for core and 2.5V for IO) Dedicated process flavors for high performance and for low power Bipolar SiGe-C NPN transistors: High Speed NPN with Ft=320GHz Medium Voltage NPN with Ft=180GHz, and High Voltage NPN Temperature range: -40°C to 175°C Dual-damascene copper for interconnect, low-k dielectric 8 Cu metal layers for interconnect Ultra-thick Cu top metal (3.0 micron) Low k inter-level dielectric MiM capacitors & Fringe MoM capacitors Thin Film Resistors (RFR) Millimiter-wave inductors Analog / RF capabilities Various power supplies supported: 2.5V, 1.2V, 1V Standard cell libraries (more than 700kgates/mm² for high speed gates, more than 970kgates/mm² for high density gates) Embedded memory (Single port RAM / ROM / Dual Port RAM)
Design kits version	2.8.a (Jul.-18)
DK front-end/back-end tools	Cadence IC 6.1.7
DK simulation tools	Spectre (Cadence), Hspice (Synopsys), GoldenGate (Keysight)
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*



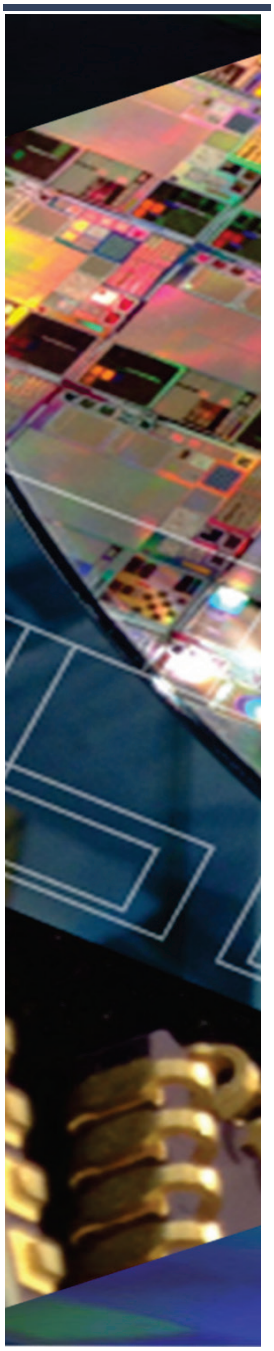
Double Polysilicon Self-Aligned (DPSA) architecture featuring a Selective Epitaxial Growth (SEG) of the base

Contact:

Jean-François PAILLOTIN
Lead Manager MPW Run/
STMicroelectronics
Jean-Francois.Paillotin@mycmp.fr

DK support contact:
cmp-support@mycmp.fr

Technology overview



Contacts:

Romain VERLY
MPW Run Manager
Romain.Verly@mycmp.fr

Jean-François PAILLOTIN
Lead Manager MPW Run/
STMicroelectronics
Jean-Francois.Paillotin@mycmp.fr

DK support contact:
cmp-support@mycmp.fr

65nm CMOS LPGP (Low Power and General Purpose)

The CMOS65LPGP technology has been introduced as general purpose and low power process to address 1.0V and 1.2V applications with 1.2V, 1.8V, 2.5V and 3.3V capable I/Os. The design kit has a large bench of fully characterized devices. The RF kit includes inductors, varactors and MiM capacitors.

TECHNOLOGY: CMOS065	STMicroelectronics IC 65nm CMOS065 Advanced CMOS
Process characteristics	CMOS gate length: 65nm drawn poly length Deep Nwell and Deep Trench Isolation Triple Vt MOS transistors (LVT, RVT and SVT) Low Power and General Purpose MOS transistors Dual gate oxide (1.0V for core and 2.5V for IO) Dedicated process flavors for high performance and for low power Temperature range: -40°C to 175°C Dual-damascene copper for interconnect, low-k dielectric 7 Cu metal layers for interconnect Low k inter-level dielectric MiM capacitors & Fringe MoM capacitors Inductors Analog / RF capabilities Various power supplies supported: 2.5V, 1.2V, 1V Standard cell libraries (more than 800kgates/mm2) Embedded memory (Single port RAM / ROM / Dual Port RAM)
Design kits version	5.8 (Jul.-19)
DK front-end/back-end tools	Cadence IC 6.1.6
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*

130nm technologies

CMP offers a wide range of technologies in the 130nm node for General purpose, millimeterwave and mixed digital and analog designs. Three 130nm technologies are offered at CMP :

- BiCMOS9MW SiGe 6ML
- HCMOS9-SOI FEM 4ML
- HCMOS9A 4ML

Hereafter, the presentations of each 130nm technologies:

BiCMOS9MW SiGe 6ML

The BiCMOS9MW technology was defined by using the 130 nm HCMOS9 as base process and adds additional levels, in front-end and back-end. It has been introduced to address millimeterwave applications (Frequencies up to 77 GHz), wireless communication (around 60GHz for WLAN), and optical communications systems.
HCMOS9GP designs can be submitted with the design kit BICMOS9MW.
Characteristics are available on our Web site.

TECHNOLOGY: BiCMOS9MW	STMicroelectronics IC 130nm BiCMOS9MW BiCMOS SiGe
Process characteristics	CMOS Gate length: 130nm drawn, 130nm effective Deep Nwell and Deep Trench Isolation Double Vt transistor offering (Low Leakage , High Speed) Dual gate oxide (1.2V for core and 2.5V for IO) Threshold voltages (for 2 families above): VTN = 450/340mV, VTP = 395/300mV Isat (for 2 families above): TN @ 1.2V: 535/670uA/mic TP @ 1.2V: 240/310uA/mic Bipolar SiGe transistors: High Speed NPN Medium VoltageNPN Typical beta (for 2 families above): 1000/1000 Typical Ft (for 2 families above): 230/150GHz Power supply 1.2V Temperature range: -40°C to 175°C 6 Cu metal layers Low k inter-level dielectric MIM capacitors Standard cell libraries (more than 180kgates/mm2) Embedded memory (Single port RAM / ROM / dual port RAM).
Design kits version	2.9.b (Apr.-17)
DK front-end/back-end tools	Cadence IC 6.1.6
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*

Technology overview

HCMOS9-SOI FEM 4ML

This technology is intended to serve at best RF ultra low cost applications. Dedicated engineering runs in H9-SOI-FEM are still possible to fabricate.

H9-SOI-FEM is built on the same solid basis of the previous standard H9SOI technology and with it shares the robustness, the capability to address all FEM (stand for Front End Module) applications (RF Switches, PA, LNA) and the expertise in RF SOI process. Nevertheless, H9-SOI-FEM technology includes several improvements such as cost-driven application, performance improvement and a better manufacturing capacity. Below, this information and characteristics are available on our web site:

TECHNOLOGY: H9SOI-FEM	STMicroelectronics IC 130nm H9SOI-FEM Advanced CMOS SOI
Process characteristics	CMOS gate length: 130nm SOI wafers with high resistive substrate 2.5V Body Contacted CMOS Floating Body CMOS 5.0V NLDMOS PLDMOS 1.2V High Speed 130nm CMOSmeta Temperature range: -40°C to 175°C 4 metal layers for interconnect Ultra-thick Cu top metal (4.0 micron) High Linearity MIM capacitor Standard cell libraries
Design kits version	14.1 (2016)
DK front-end/back-end tools	Cadence IC 6.1.6
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*
Typical Turnaround time	Typical leadtime: 16-18 weeks from MPW run deadline to packaged parts

The design kit is provided with fully characterized devices:

		Switches	Antenna Tuning	PA	DCDC	Hx Filters	LNA
MOS Transistors (Floating & Body Contacted)	2.5V GO2 Body Contacted CMOS	x	x	x	x	x	
	2.5V GO2 Floating Body CMOS	x	x	x	x	x	
	2.5V GO2 BC/FB RF NMOS (RonCoff)	x	x				
	1.2V GO1 High Speed CMOS (BC & FB)						x
Capacitors	MIM2 Capacitance	x	x	x	x	x	
	MOM RF Capacitance	x	x	x	x	x	
	N+ Poly/NWELL 6 fF/um²	x	x				
High Voltage Transistors	NLDEMOS_HP (Ft 36GHz, BVds 13V)			x	x		
	PLDEMOS_HP (Ft 19GHz, BVds 8V)				x		
Inductances Family	High Current/ High Q Pcells			x	x	x	
Resistors	Silicided N+ Poly 10 ohms/sq	x					
	Unsilicided P+ Poly 320 ohms/sq	x					
	High value poly resistor RHipo 1Kohms/sq (option)	x		x	x	x	
Diodes	Lateral P+/Nwell non-gated diodes (ESD)	x					
	N+/Pwell non gated diode (Bandgap)	x					
		P1 perimeter		P2 perimeter			P3 perimeter

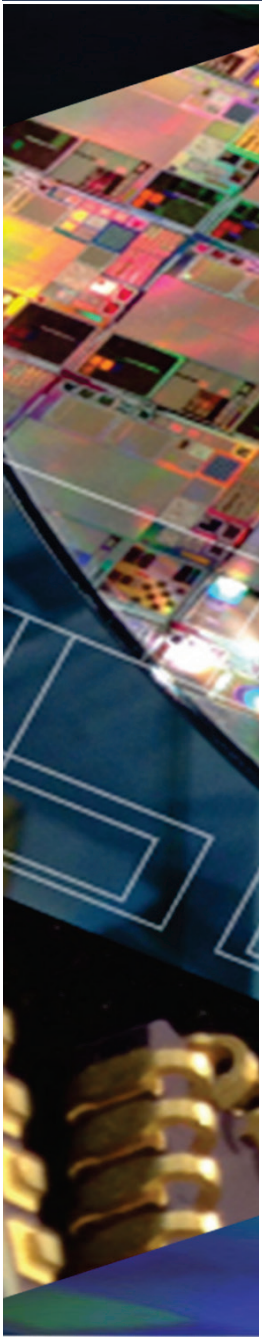
Contacts:

Romain VERLY
MPW Run Manager
Romain.Verly@mycmp.fr

Jean-François PAILLOTIN
Lead Manager MPW Run/ STMicroelectronics
Jean-Francois.Paillotin@mycmp.fr

DK support contact:
cmp-support@mycmp.fr

Technology overview



HCMOS9A 4ML

This STMicroelectronics technology on the 130nm node, based on the HCMOS9GP DRM, targets the mixed digital analog design with energy management features. Dedicated engineering runs in pure HCMOS9A are still possible to fabricate.

TECHNOLOGY: HCMOS9A	STMicroelectronics IC 130nm HCMOS9A CMOS High Voltage
Process characteristics	CMOS gate length: 130nm drawnpoly length Deep Nwell and Deep Trench Isolation Vt transistor offering (Low Power, Analog) Threshold voltages (for 2 families above): VTN = 700/697mV, VTP = 590/626mV Isat (for 2 families above): TN: 280/658uA/um TP: 104/333uA/um Bipolar NPN transistors Typical beta: 90 Ft Max @ Vbc=0: 2,4GHz 2 specific implant levels: NDRIFT & PDRIFT MIM 5fF/µm2 Double gate oxide for analog features Temperature range: -40°C to 175°C 4 metal layers in standard Fluorinated SiO2 Inter Metal dielectrics Power supply: 1. 2V for Digital, 4.6V for Analog application Multiple Standard cell libraries. Note: HCMOSA process from STMicroelectronics is presently mainly used for making the OxRAM post-process from CEA-LETI in order to make embedded. The metal stack back-end from the ST process is stopped at the last metal layer to allow the [OxRAM / NVM->datasheet38] post-process deposition by CEA-LETI. All HCMOSA MPW runs are presently offered with this NVM post-process. Nevertheless, dedicated engineering runs in pure HCMOS9A are still possible to run
Design kits version	10.9 (May-19)
DK front-end/back-end tools	Cadence IC 6.1.7
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*

The design kit is provided with fully characterized devices:

HV MOS

- N+ Poly/ 8.5 nm
- N&P 8.5 nm Gate Oxide 20 V Drift MOS - Extra masks : NDRIFT & PDRIFT
- N&P 8.5nm Gate oxide 10V Drift MOS

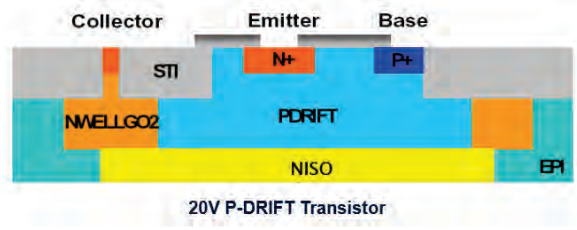
Bipolar Transistors

- NPN Bipolar N+/ Pdrift/ NISO - Extra mask : PDRIFT
- PNP

Capacitor

- N+ Poly/ 8.5 nm Gate Oxide/ Nwell GO2
- MOM Capacitor
- Plate capacitor

MIM5 Capacitor.



20V P-DRIFT Transistor

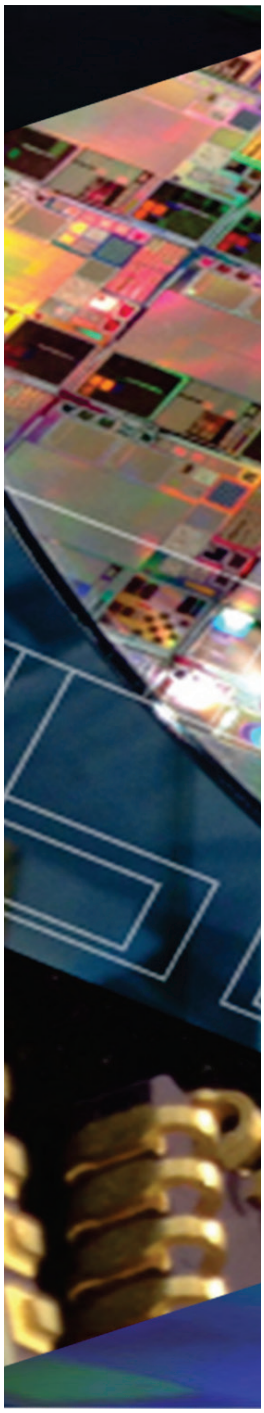
Contacts:

Romain VERLY
MPW Run Manager
Romain.Verly@mycmp.fr

Jean-François PAILLOTIN
Lead Manager MPW Run/
STMicroelectronics
Jean-Francois.Paillotin@mycmp.fr

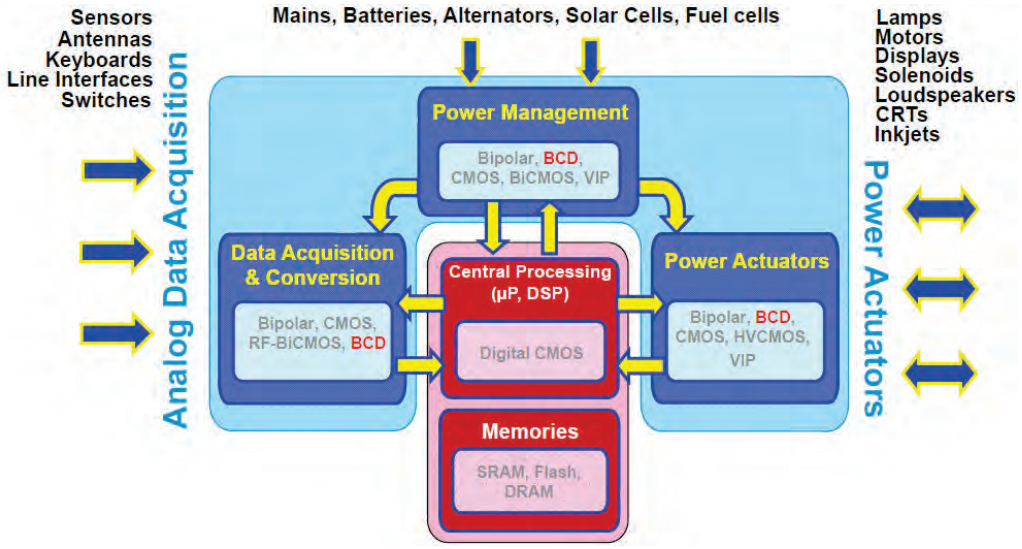
DK support contact:
cmp-support@mycmp.fr

Technology overview



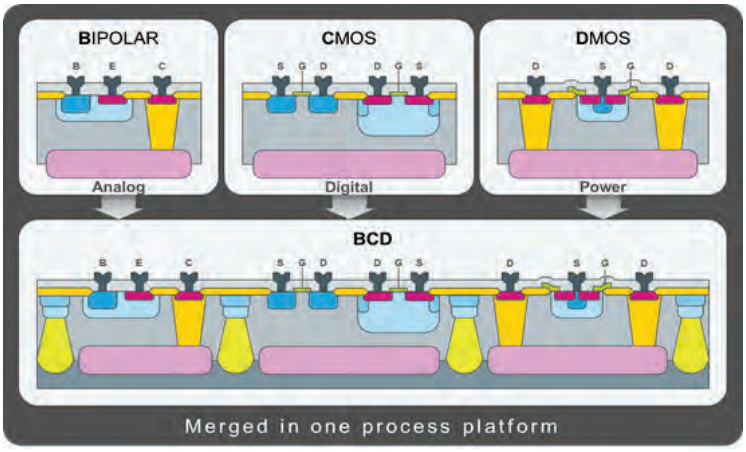
0.16µm BCD8Sp Bipolar-CMOS-DMOS 4ML

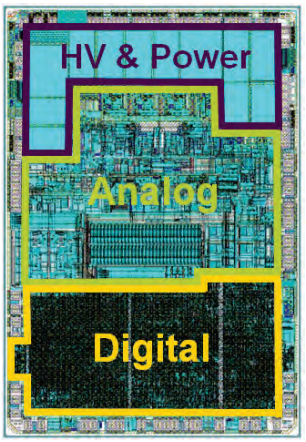
ST Microelectronics « Smart Power » BCD8sP technology combines high power transistors with low power digital and analog devices on a single chip. This technology is dedicated to power management systems, power supplies, motor drivers, amplifiers etc.



BCD in Electronic System Partitioning, Courtesy of ST Microelectronics

TECHNOLOGY: BCD8sP	STMicroelectronics IC 0.16µm BCD8sP BCD High Voltage
Process characteristics	Temperature range: 40°C to +175°C 0.16µm Bipolar-CMOS-DMOS 4 metal layers (2 top metal options : Al or CuRDL) Baseline 1.8V CMOS Power devices: 5V / 10V / 18V / 27V / 42V / 60V Dual gate oxide process: 1.8V CMOS, 5V CMOS & Power Devices Optional DTI for lateral isolation
Design kits version	2.4 (2016)
DK front-end/back-end tools	Cadence IC 6.1.6
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*





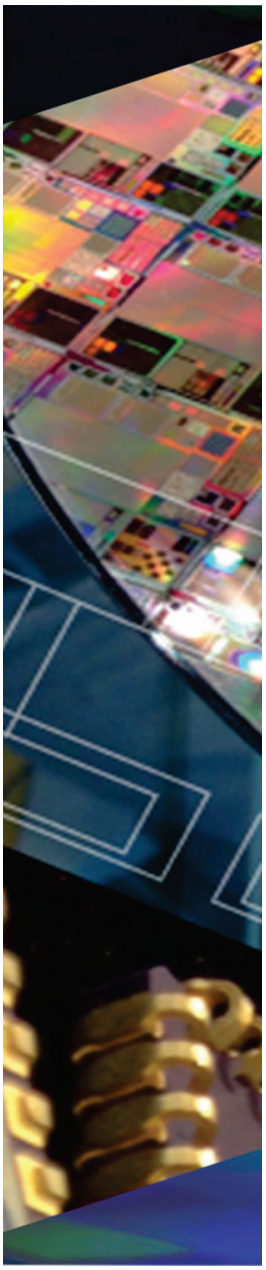
Analog + Digital + Power & HV on one chip : Courtesy of STMicroelectronics

Contact:

Lyubomir KERACHEV
Technical Manager
Lyubomir.Kerachev@mycmp.fr

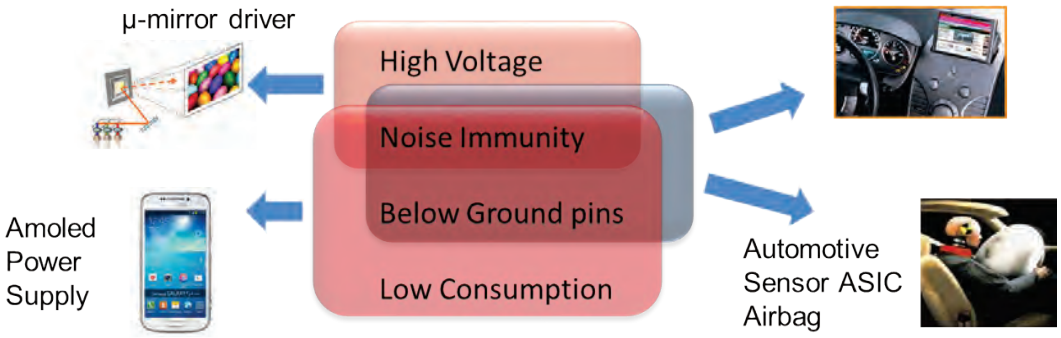
Kit support contact:
cmp-support@mycmp.fr

Technology overview



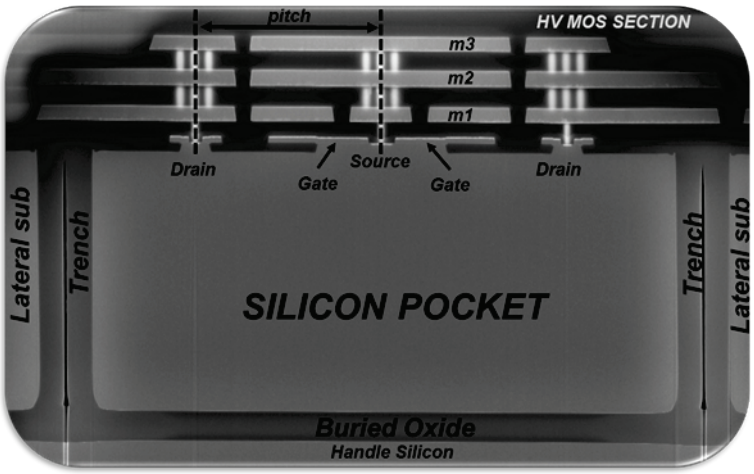
0.16µm BCD8s-SOI High Voltage Bipolar-CMOS-DMOS 4ML

ST Microelectronics « Smart Power » BCD8s-SOI technology is dedicated to high voltage applications on SOI substrates. This technology is convenient and even mandatory in case of MEMS & micro-mirror driver, consumer and automotive audio amplifiers, automotive sensor interface, 3D Ultrasound etc.



Fully isolated HV MOS cross section

TECHNOLOGY: BCD8s-SOI	STMicroelectronics IC 0.16µm BCD8s-SOI BCD SOI High Voltage
Process characteristics	Temperature range: -40°C to +175°C 0.16µm Bipolar-CMOS-DMOS 4 Metal Levels with last Al Thick Power metal Baseline 3.3V CMOS Medium Voltage Module: 6V / 20V / 40V NMOS and PMOS High Voltage Module: 70V / 100V / 140V / 200V NMOS and PMOS Optional 2nd gate oxide for 1.8V CMOS Dielectric Isolation on SOI Available memory: OTP
Design kits version	2.1 (2017)
DK front-end/back-end tools	Cadence IC 6.1.7
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*



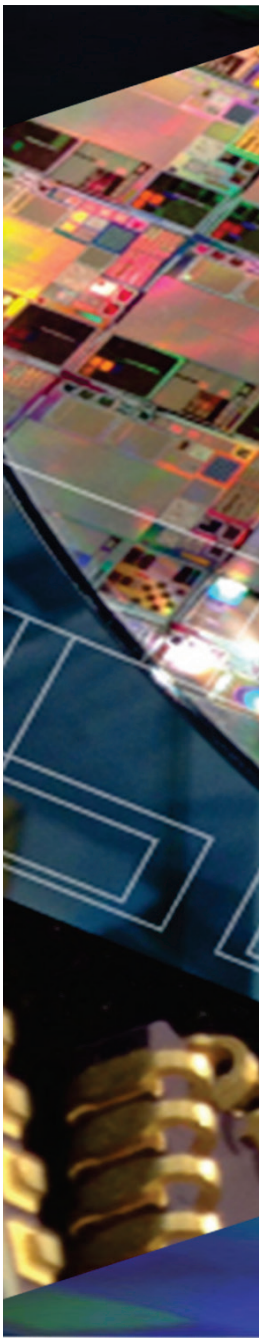
Fully isolated HV MOS section

Contact:

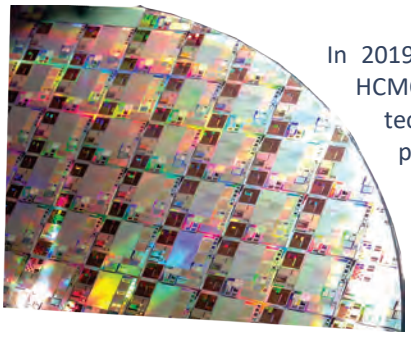
Lyubomir KERACHEV
Technical Manager
Lyubomir.Kerachev@mycmp.fr

Kit support contact:
cmp-support@mycmp.fr

Technology overview



IRT NanoElec CEA LETI

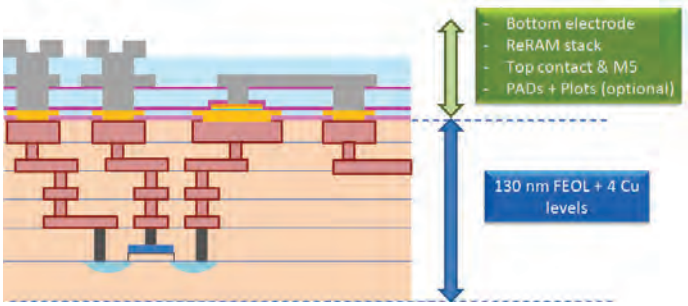


In 2019, CMP will provide access to HCMOS9A ST Microelectronics technology coupled with CEA-LETI post-process OxRAM Non volatile memory.

This technology targets the mixed digital-analog designs integrating energy harvesting features. The back-end process is provided by at STMicrolectronics but stops at the last metal layer to allow the post-process at CEA-LETI. This post-process allows integration of additional layers at wafer level for NVM deposition.

MAD200 OxRAM CMOS Non Volatile Memory (NVM)

TECHNOLOGY: Memory Advanced Demonstrator 200mm (MAD200)	**IRT Nanoelec/LETI-CEA MAD200 Memory Advanced Demonstrator 200mm CMOS NVM**
Process characteristics	In order to address new emerging Non Volatile Memory technologies and to develop an optimized memory stack that targets the client requests, CEA-LETI with CMP offers also a so-called Memory Advanced Demonstrator (MAD) Multi-Project Wafer based on 130 nm 200mm base wafers with 4 copper metal lines. The memory module, that can consist of OxRAM technology, is fabricated in the BEOL before pad level. This versatile test vehicle offers the possibility to have on the same silicon test structures spanning from simple resistors (1R), resistors with its selector transistor (1T1R), memory arrays (1kb cuts to 1Mb array) up to complex IC designs allowed by the routing placed on the 4 metal levels. All such structures are essential for a deep analysis of the memory functionality: from bulk material (with its interfaces) screening, obtained by the 1R and 1T1R; passing through statistical analysis of extrinsic bits, obtained by memory arrays; up to first validation of complex functions obtained by specific designs. MAD offers also a benchmark opportunity between different technologies (PCM, MRAM, CBRAM, ...) with the same test vehicle in order to extract benefits and drawback from each of them.
Application area	Storage Class memory, Embedded memory, Neuromorphic, Computing, Artificial Intelligence accelerator.
Design kits version	10.9-10-Addon_NVM_H9A@2018.4.1 (May-19)
DK front-end/back-end tools	Cadence IC (release aligned on ST HCMOS9A PDK)
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*
Typical Turnaround time	Typical leadtime: 24 weeks from MPW run deadling to packaged parts delivery



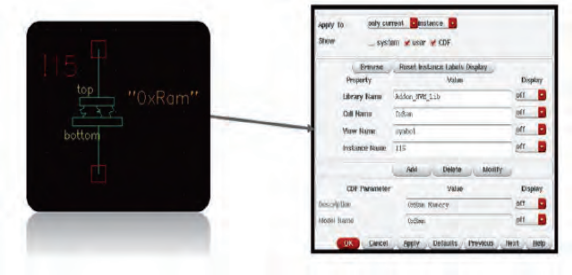
MAD cross-section

The full platform's highlights:

200mm STMicroelectronics HCMOS9A base wafers in 130nm node

- All routing is made on ST base wafers from M1 to M4 (included)
- Leti's OxRAM memory module is fabricated on top
- One level of interconnect (i.e. M5) plus pads are fabricated in Leti's cleanroom.

Library name: Addon_NVM_LibCategory Device: OxRAM



CONTENT OF NVM ADDON:

Librairie de devices:
- OxRAM (symbol, CDF, pcell)

Simulation électrique:
- Modèles SPICE
- Fichier technologique

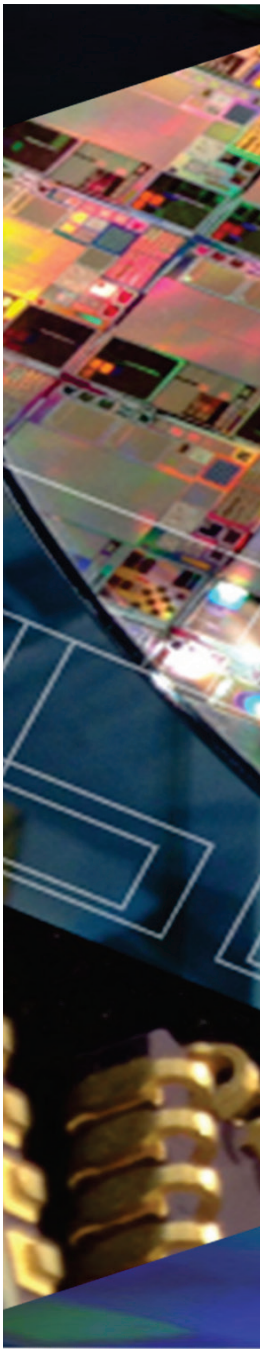
Vérification physique:
- DR/LVS incrémentalLayout finishing:
  - Dummies génération
  - DRC Density

Contact:

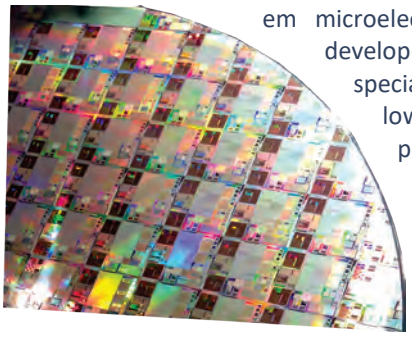
Romain VERLY
MPW Run Manager
Romain.Verly@mycmp.fr

DK support contact:
cmp-support@mycmp.fr

Technology overview



em microelectronic



em microelectronic Electronic Marin (em) is a Swiss developer and semiconductor manufacturer specialized in the design and the production of ultra-low power and low voltage integrated circuits for battery-operated and field-powered applications in consumer, automotive and industrial areas. Its products include RFID circuits, smart cards ICs, ultra-low power microcontrollers, power management, LCD divers and displays, sensor and optoelectronic ICs etc. The company has its headquarters at Marin, near Neuchâtel, in Switzerland

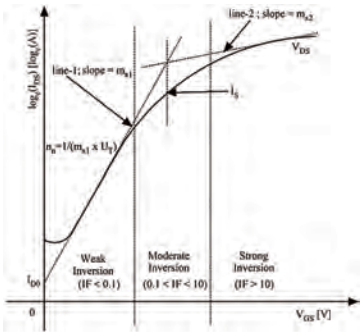
em 0.18µm CMOS EMALPC18 logic

CMP is now offering to its users an access to one of em mainstream technologies ALP018. This is a 0.18µm CMOS process node developed and optimized in house for low current (nA bias) and low voltage operations (down to 0.4V). It is suitable for analog (low leakage and low noise) and mixed-signal designs (digital functions with densities of up to 100kGates/mm^2).

The design kit offers large choice of IP libraries optimized for low power and low voltage, and input/output pads with low-leakage ESD protection. Non-volatile memory blocks for trimming and storage are also available. Reliable simulation results are achieved for near/sub threshold voltage operations thanks to the accurate EKV models.

The design kit is organized around the Cadence framework and its Virtoso suite but it also includes Synopsys tools such as CustomSim for analog and mixed signal simulation and PrimeTime for static timing analysis.

TECHNOLOGY: EMALPC18	em microelectronic IC em microelectronic 0.18µm CMOS EMALPC18 logic CMOS
Process characteristics	Met. layers: 4/5. Option B 4ML or Option M -5ML Minimum Gate length: 180nm [drawn] Dual Gate Oxides: 3.0nm ThinGOX [1.98V max] and 6.5nm DualGOX [3.63V max] FEOL isolation: Non Epi or p-Epi substrate [16-24Ω.cm], STI [Shallow trench isolation] Supply voltage: 1.8V or 3.3V
Application area	Ultra-Low Power, Ultra-Low Voltage Analog Designs (low leakage, low noise, pairing) Mixed signal (100kGates/mm2) Low current (nA bias), Low voltage (down to 0.4V)
Design kits version	0.7
DK front-end/back-end tools	Cadence IC 6.1.7
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*



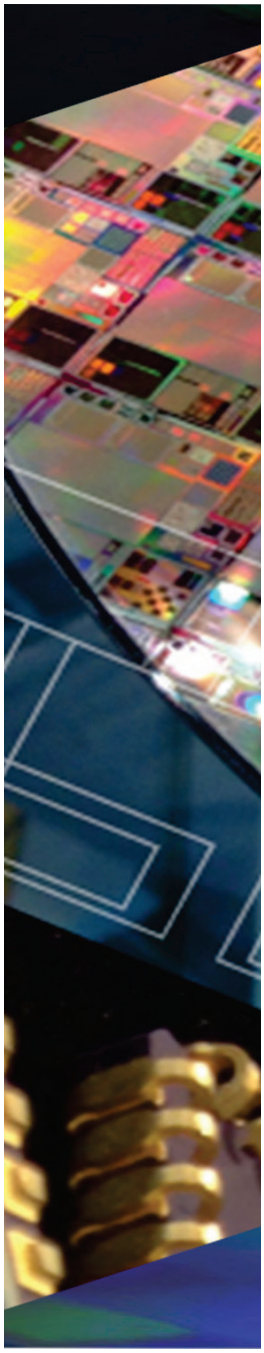
Contacts:

Lyubomir KERACHEV
Technical Manager
Lyubomir.Kerachev@mycmp.fr

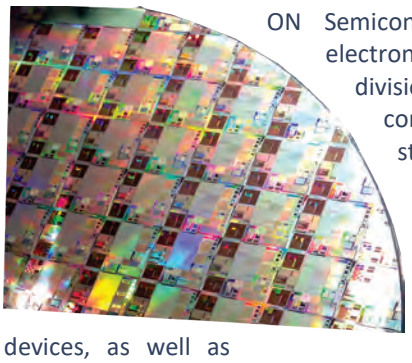
Nicolas PARTENZA
MPW Run Manager
Nicolas.Partenza@mycmp.fr

DK support contact:
cmp-support@mycmp.fr

Technology overview



ON Semiconductor



ON Semiconductor is an American manufacturer of electronic dies born in 1999 from the semiconduc-tor division of the telecommunications giant Motorola. Although the company still today provides its former parent company with the standard discrete analog and digital components needed to manufac-ture its products, ON Semiconductor also very early pursued an active policy of business-building to currently generate a turnover of 6 billion dollars and to employ 36,000 people around the world. Its portfolio of solutions includes power management, signal processing, and connectivity devices, as well as sensors, chip systems, and other custom-built solutions that make ON Semiconductor one of the leaders in the manufacturing of high voltage integrated circuits.

ON 0.18µm CMOS ONC18MS

The 0.18µm technology is a platform dedicated to the design and the manufacturing of high-voltage, high-integration density, mixed signal circuits, ideal for addressing a wide range of applications in the automotive, medical and defense industries.

The base process offers two operating voltages (1.8 and 3.3V) and 6 interconnection levels. The asso-ciated design kit provides access to numerous components such as MIM capacitors, resistors, Zener and Schottky diodes, and bipolar transistors, plus a wide range of memory functions (SRAM, ROM, EEPROM and OTP). Several process options are also available such as salicidation and die stitching.

TECHNOLOGY: ONC18MS	**ON Semiconductor IC ON Semiconductor 0.18µm CMOS ONC18MS CMOS**
Process characteristics	Met. layer(s): 5, thick top metal Poly layer(s): 1 Maximum die size: stitching options for larger dies Available I/O: I/O standard cell libraries for core and pad limited designs, with internal level shifters, for various voltages Temp. range: -45°C/+135°C Supply voltage: 1.8V/3.3V Memory options: single port SRAM dual port SRAM ROM non-volatile memory One-Time Programmable (OTP)
Application area	Highly integrated high voltage mixed signal processes ideal for many automotive, industrial, medical and defense applications
Design kits version	1.32p2
DK front-end/back-end tools	Cadence IC 6.1.7
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*

ON 0.18µm HV-CMOS ONC18-I4T

The I4T technology is based on the previously described process, but uses an epitaxial substrate and shallow trench isolation to insulate areas polarized up to 120V. Many high-voltage MOS and bipolar transistors and diodes are added to the components available in the design kit. In particular, the user has the choice between two options according to the maximum voltage he intends to apply to the drain of the MOS transistors: the i45 option, which gives access to nLDMOS transistors supporting up to 45V, and the i70 option which, with the addition of two masking steps, allows to reach 70V. Note that it is not possible with I4T technology to make deep wells, and some NPN and RF transistors which use this type of wells by construction are therefore not available.

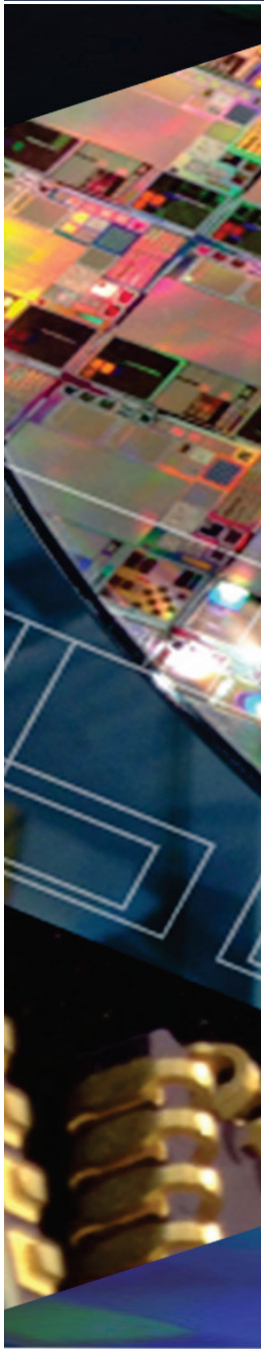
Contacts:

François BERTHOLLET
MPW Run Manager
Francois.Berthollet@mycmp.fr

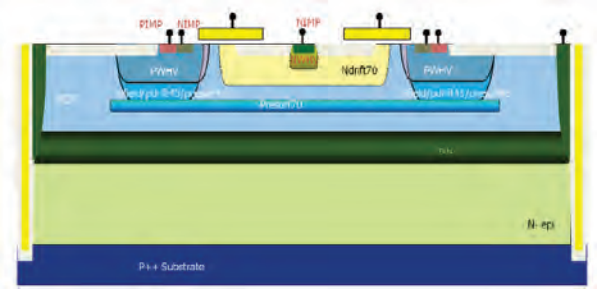
Lyubomir KERACHEV
Technical Manager
Lyubomir.Kerachev@mycmp.fr

DK support contact:
cmp-support@mycmp.fr

Technology overview



TECHNOLOGY: ONC18I4T	ON Semiconductor IC ON Semiconductor 0.18µm CMOS HV ONC18I4T CMOS High Voltage
Process characteristics	Met. layer(s): 5, thick top metal Poly layer(s): 1 Maximum die size: stitching options for larger dies Available I/O: I/O standard cell libraries for core and pad limited designs, with internal level shifters, various voltages Bipolar transistors: HV and LV Parasitic High Voltage devices: HV 70V DMOS Temp. range: -45°C/+200°C Supply voltage: 1.8V/3.3V Memory options single port SRAM dual port SRAM ROM non-volatile memory One-Time Programmable (OTP)
Application area	High-voltage automotive applications thanks to Deep Trench Isolation (DTI) Also serves as a platform for highly integrated high voltage mixed signal processes ideal for many industrial applications
Design kits version	1.32p2
DK front-end/back-end tools	Cadence IC 6.1.7
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*



Deep trench isolation for compact HV devices 0.18µm I4T70

ON 0.35µm CMOS ONC35U

The base process, called ONC35U, is presented as the ideal solution in 0.35µm node to conceive and manufacture at low cost mixed-signal circuits with simple and effective digital functions. Optimized to operate at 3.3V, it offers the opportunity to work up to 5V, provides 5 levels of metallization and has a range of memory options as developed as for 0.18µm technologies.

TECHNOLOGY: ONC35U	ON Semiconductor IC ON Semiconductor 0.35µm CMOS ONC35U CMOS
Process characteristics	Met. layer(s): 4, thick top metal Poly layer(s): 2 Maximum die size: : stitching options for larger dies Available I/O: I/O standard cell libraries for core and pad limited designs, 5V tolerant Temp. range: -40°C/+150°C Supply voltage: 3.3V/5V memory options: Asynchronous single port SRAM Asynchronous dual port SRAM Asynchronous diffusion ROM EEPROM
Application area	Mixed signal designs requiring a moderate amount of digital logic (up to 250k gates)
Design kits version	1.5
DK front-end/back-end tools	Cadence IC 6.1.6
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*

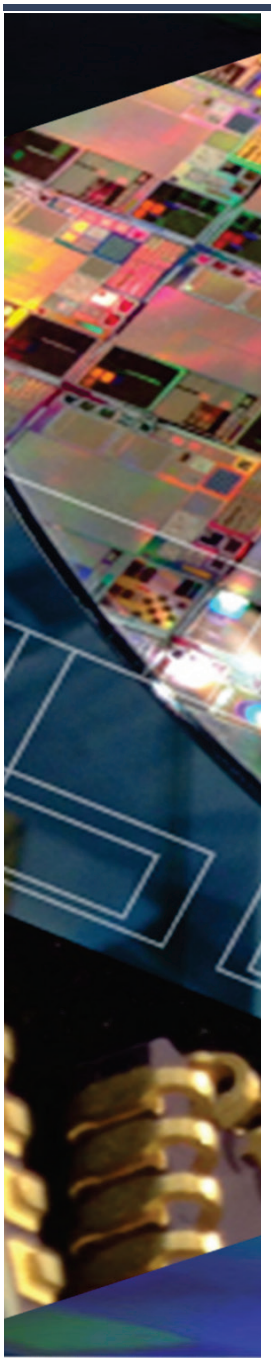
Contacts:

François BERTHOLLET
MPW Run Manager
Francois.Berthollet@mycmp.fr

Lyubomir KERACHEV
Technical Manager
Lyubomir.Kerachev@mycmp.fr

DK support contact:
cmp-support@mycmp.fr

Technology overview

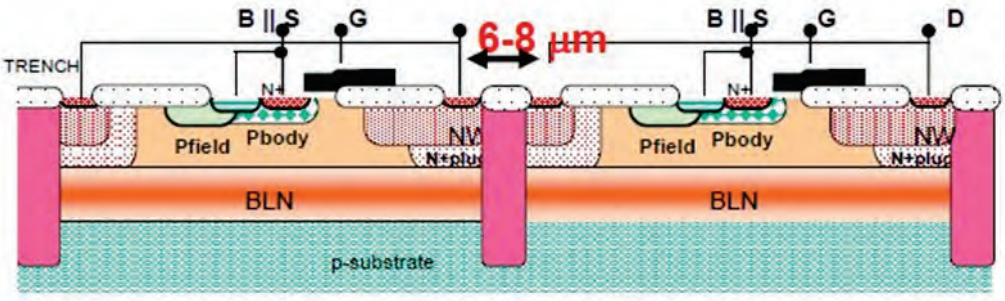


ON 0.35µm HV-CMOS ONC35-I3T25U & ON 0.35µm HV-CMOS ONC35-I3T50U

The other two technologies, the ONC35-I3T25U and ONC35-I3T50U, are clearly oriented towards high-voltage applications by offering two operating voltages (3.3 and 12V), and a wide choice of MOS tran-sistors which can support up to 25V on the drain for the I3T25U and 50V for the I3T50U. The user may also use MIM capacitors, resistors, and Zener and Schottky diodes.

TECHNOLOGY: ONC35I3T25U	ON Semiconductor IC ON Semiconductor 0.35µm CMOS HV ONC35I3T25U CMOS High Voltage
Process characteristics	Met. layer(s): 4, thick top metal Poly layer(s) : 2 Available I/O : I/O standard cell libraries for core and pad limited designs Temp. range : -40°C/+155°C Supply voltage : 3.3V/12V Memory options: Synchronous high speed/high temp single port SRAM Synchronous high speed/high temp dual port SRAM Low power synchronous SRAM Synchronous high speed/high temp diffusion ROM Low power synchronous via programmable ROM One-Time Programmable (OTP) EEPROM (no additional masks or processing steps)
Application area	Calibre PEX
Design kits version	1.5
DK front-end/back-end tools	Cadence IC 6.1.6
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*

TECHNOLOGY: ONC35I3T50U	ON Semiconductor IC ON Semiconductor 0.35µm CMOS HV ONC35I3T50U CMOS High Voltage
Process characteristics	Met. layer(s): 4, thick top metal Poly layer(s): 1 Available I/O: I/O standard cell libraries for core and pad limited designs, 5V tolerant Temp. range: -40°C/+190°C High Voltage devices: up to 40V Digital and analog supply voltage: 3.3V Memory options Synchronous high speed/high temp single port SRAM Synchronous high speed/high temp dual port SRAM Low power synchronous SRAM Synchronous high speed/high temp diffusion ROM Low power synchronous via programmable ROM One-Time Programmable (OTP) EEPROM (no additional masks or processing steps)
Application area	Increased digital content in a mixed signal and/or high voltage environment 3 and 5 metal layers options (thick top metal) Additional options on request: MiM capacitor, HIPO, Polyimide
Design kits version	1.5
DK front-end/back-end tools	Cadence IC 6.1.6
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*



I3T50 cross section

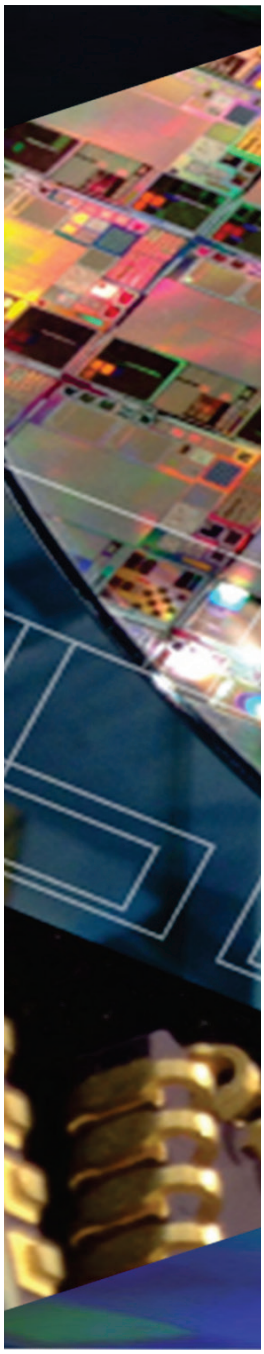
Contacts:

François BERTHOLLET
MPW Run Manager
Francois.Berthollet@mycmp.fr

Lyubomir KERACHEV
Technical Manager
Lyubomir.Kerachev@mycmp.fr

DK support contact:
cmp-support@mycmp.fr

Technology overview



ams

CMP offers ams technologies since 1987. Based in Austria, ams is an analog IC company that develops and manufactures high performance semiconductors. ams' products are aimed at applications which require extreme precision, accuracy, dynamic range, sensitivity, and ultra-low power consumption. ams' product range includes sensors, sensor interfaces, power management ICs and wireless ICs for customers in the consumer, industrial, medical, mobile communications and automotive markets.

0.35µm C35B4C3 CMOS DLP/4LM 3.3V/5V

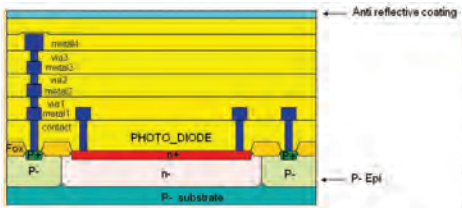
This process is used for digital, analog and mixed applications but also for high frequency applications. 0.35µm CMOS technology offers four metal layers, digital standard cells and bulk micromachining. The bulk micromachining post process allows MEMS integrated togehter with electronic components.

TECHNOLOGY: C35B4C3	ams IC 0.35µm C35B4C3 CMOS
Process characteristics	Met. layer(s): 4 Poly layer(s): 2, high resistive poly Maximum die size: 2cm x 2cm DLP Usable cells: about 300 digital cells Available I/O: I/O cell library with digital pads is available 3.3V, 3V/5V, 5V with internal level shifters Temp. range: -40° C. / +125° C. Supply voltage: 5V or 3.3V
Application area	Mixed signal analog digital, large digital designs, system on chip
Design kits version	4.10 ISR 15 (Nov.-17)
DK front-end/back-end tools	Cadence IC 6.1.6
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*

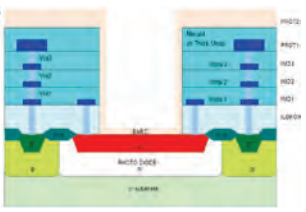
0.35µm C35B4O1 CMOS Opto ARC and C35B4OA CMOS Opto BARC

Based on the CMOS process C35B4C3, the process offers additional options of epitaxial wafers and anti-reflective layer. This is available both for C35B4O1 and C35B4OA. The only difference between them is the use of a deep etching in C35B4OA making more efficient the optical absorbtion.
Applications: Photo sensors, APS, CMOS Camera …

TECHNOLOGY: C35B4O1	ams IC 0.35µm ARC C35B4O1 CMOS Opto ARC
Process characteristics	This 0.35 CMOS-Opto process is offered in each 0.35 CMOS run (C35B4C3). This is a ARC (Anti Reflective Coating) option. Anti-Reflective Coating (ARC) allows a higher photo-sensitivity than C35B4C3. P-Epi wafers for lowering current leakage in the diode (lower dark current). The C35B4O1 is with 4 layers metal available for prototyping and low volume production. Met. layer(s): 4 Poly layer(s): 2 Maximum die size: 2cm x 2cm DLP Usable cells: about 300 digital cells Available I/O: I/O cell library with digital pads is available 3V, 3V/5V, 5V with internal level shifters Temp. range: -40° C. / +125° C. Supply voltage: 5V or 3.3V.
Application area	Provides enhanced optical sensitivity for embedded photodiodes and high density CMOS camera products
Design kits version	4.10 ISR 15 (Nov.-17)
DK front-end/back-end tools	Cadence IC 6.1.6
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*



CMOS OPTO Process



BARC process option cross section

Contacts:

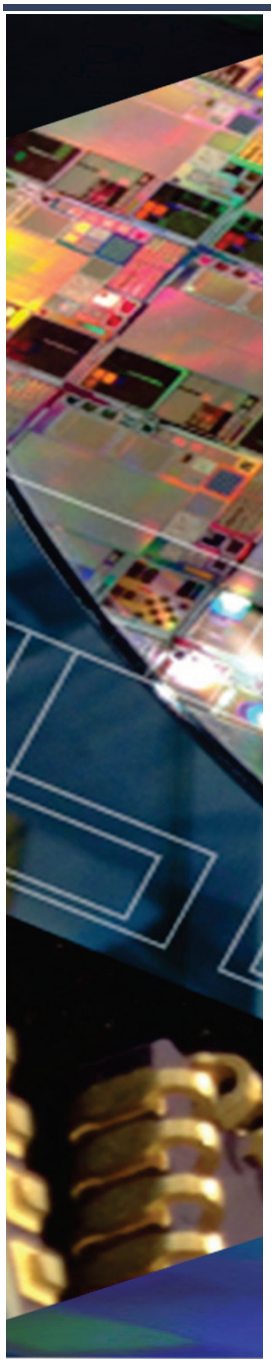
Lyubomir KERACHEV
Technical Manager
Lyubomir.Kerachev@mycmp.fr

François BERTHOLLET
MPW Run Manager
Francois.Berthollet@mycmp.fr

Nicolas PARTENZA
MPW Run Manager
Nicolas.Partenza@mycmp.fr

DK support contact:
cmp-support@mycmp.fr

Technology overview

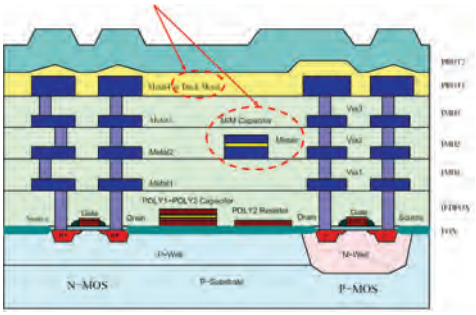


0.35µm C35B4M3 CMOS DLP/4LM ThickM4 & MIM

Based on the 0.35 CMOS standard process. There is a planarization and anti-reflective coating that allows better optical features.
This process comes with P-Epi wafers for lowering current leakage in diodes (lower dark current).
Applications: Photo sensors, APS, CMOS Camera …

TECHNOLOGY: C35B4M3	ams IC 0.35µm RF C35B4M3 CMOS RF
Process characteristics	CMOS 0.35 C35B4M3 Same as C35B4C3 with Thick Metal module instead of Metal 4 module and with MIM capacitor module Poly layer(s): 2, high resistive poly Maximum die size: 2cm x 2cm Usable cells: about 300 digital cells Available I/O: I/O cell library with digital pads is available 3V, 3V/5V, 5V with internal level shifters Temp. range: -40° C. / +125° C. Supply voltage: 5V or 3.3V
Application area	Mixed signal analog digital, large digital designs, system on chip, RF
Design kits version	4.10 ISR 15 (Nov.-17)
DK front-end/back-end tools	Cadence IC 6.1.6
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*

Thick Metal and MIM available in C35B4M3



CMOS RF Process cross section

0.35µm H35B4D3 CMOS DLP/4LM High Voltage

This process is optimized for complex mixed signal circuits up to 120V operating conditions. It comes with different MOS devices supporting different voltages, all in the same substrate : 3.3V, 5V, 20V, 50V, and 120V. Analog and digital low voltage parts from C35B4C3 can be embedded in this process.

TECHNOLOGY: H35B4D3	ams IC 0.35µm H35B4D3 CMOS High Voltage
Process characteristics	Met. layer(s): 4 Thick Metal 4 Poly layer(s): 2, high resistive poly Maximum die size: 2cm x 2cm Usable cells: about 300 digital cells Available I/O: I/O cell library with digital pads is available 3V, 3V/5V, 5V with internal level shifters. Floating digital pads available with 3.3V Temp. range: -40° C. / +125° C. Supply voltage: 3.3V, 5V, 20V, 50V, 120V (max gate voltage 5V, 20V)
Application area	Mixed signal analog digital, HV designs, system on chip
Design kits version	4.10 ISR 15 (Nov.-17)
DK front-end/back-end tools	Cadence IC 6.1.6
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*

Isolate 3.3V/5V *NMOS50V* *PMOS50V*

Contacts:

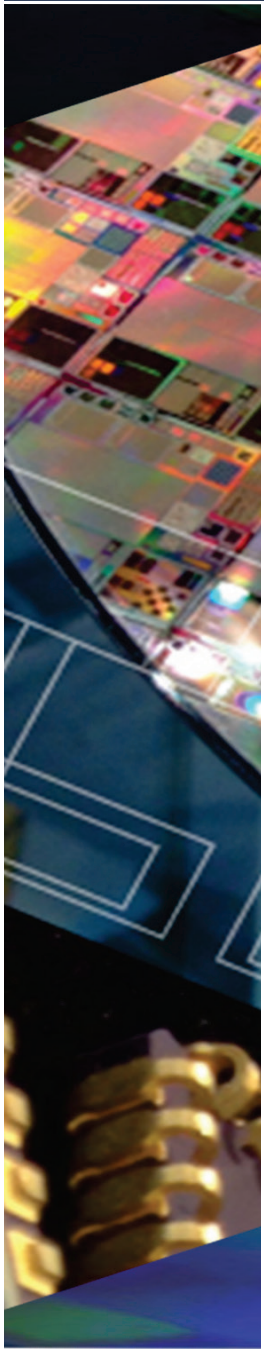
Lyubomir KERACHEV
Technical Manager
Lyubomir.Kerachev@mycmp.fr

François BERTHOLLET
MPW Run Manager
Francois.Berthollet@mycmp.fr

Nicolas PARTENZA
MPW Run Manager
Nicolas.Partenza@mycmp.fr

DK support contact:
cmp-support@mycmp.fr

Technology overview



0.35µm S35D4M5 SiGe BiCMOS DLP/4LM

This BiCMOS process is optimized for high frequencies up to several Giga-Hertz. The applications cover circuits for mobile communication to high speed networks. These advanced processes offer high-speed bipolar-transistors with excellent analog performance, such as high fmax and low noise, complementary MOS transistors, very low-parasitic linear capacitors, linear resistors and spiral inductors.

TECHNOLOGY: S35D4M5	ams IC 0.35µm S35D4M5 BiCMOS SiGe
Process characteristics	SiGe BiCMOS 0.35 S35D4M5 from ams Met. layer(s): 4, thick metal MIM capacitor Poly layer(s): 2, high resistive poly. Maximum die size: 2cm x 2cm Usable cells: about 300 digital cells Available I/O: I/O cell library with digital pads is available 3V, 3V/5V, 5V with internal level shifters Temp. range: -40° C. / +125° C. Supply voltage: 5V or 3.3V
Application area	Mixed signal analog/RF/digital, large digital designs, system on chip
Design kits version	4.10 ISR 15 (Nov.-17)
DK front-end/back-end tools	Cadence IC 6.1.6
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*

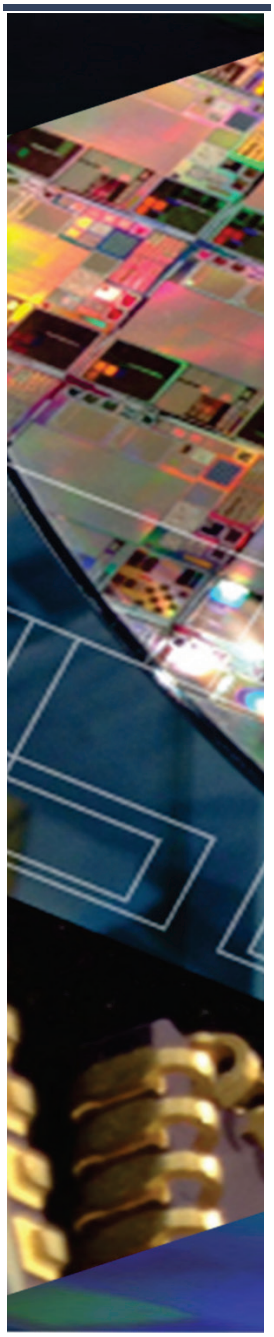
Contacts:

Lyubomir KERACHEV
Technical Manager
Lyubomir.Kerachev@mycmp.fr

François BERTHOLLET
MPW Run Manager
Francois.Berthollet@mycmp.fr

Nicolas PARTENZA
MPW Run Manager
Nicolas.Partenza@mycmp.fr

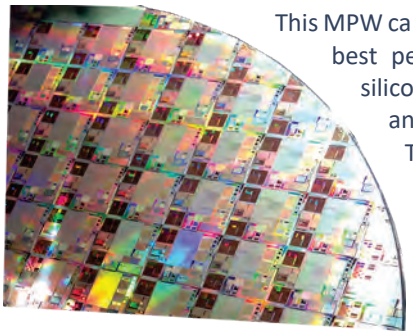
DK support contact:
cmp-support@mycmp.fr



Si-Photonic processes

In addition to ICs, CMP provides Silicon Photonic processes, for prototyping and low volume production.

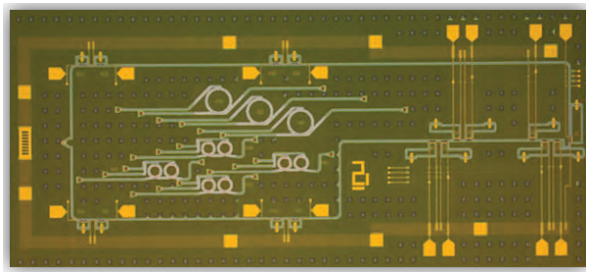
IRT Nanoelec/LETI CEA

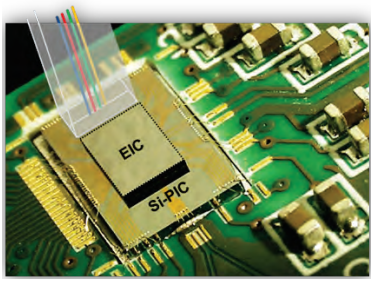


This MPW capability on 310nm SOI platform is offering the design of various best performance passive and high-speed active devices such as silicon electro-optic modulators and germanium photo-detectors and still coupled with thermal tuning capability as metal heaters. Two AlCu levels are available for more optimal routing which is also compatible for backend treatment as Under Bump Metallization.

Si310-PHMP2M

TECHNOLOGY: Si310-PHMP2M	IRT Nanoelec/LETI-CEA Silicon Photonic IC Si310-PHMP2M Silicon Photonic
Process characteristics	200mm SOI platform with 300nm Si and 800nm buried oxide Multilevel patterning to define various silicon heights of 0, 65, 165 and 300nm 2 metal layers Passive structures 1D & 2D Grating couplers Shallow, deep rib and strip waveguides & bends Active structures Lateral Ge PIN photodiode MZ and RR Modulators Multimode interferometers TiTiN Metal heater
Application area	Telecom, DataCom, ComputerCom
DK front-end/back-end tools	Cadence IC 6.1.7 DK version 2019.4 Synopsis Optodesigner DK version 2019.3.10.1
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*





Optical transceiver circuit and module, courtesy of LETI

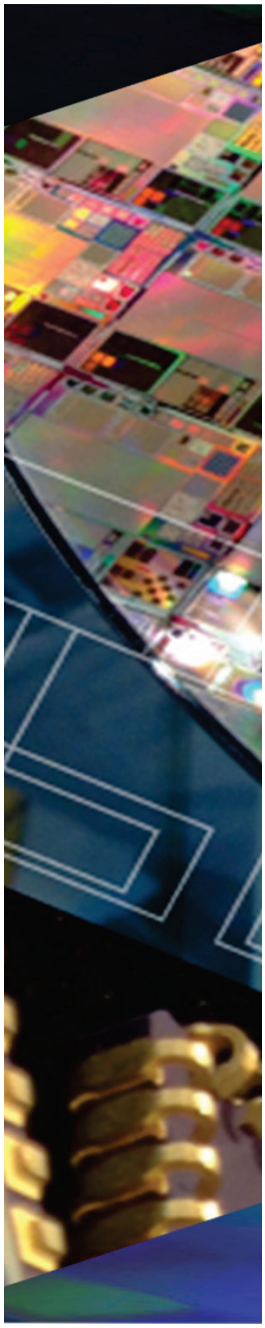
Contacts:

François BERTHOLLET
MPW Run Manager
Francois.Berthollet@mycmp.fr

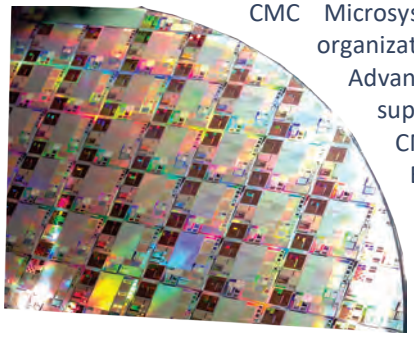
Lyubomir KERACHEV
R&D Engineer / MPW Run Manager
Lyubomir.Kerachev@mycmp.fr

DK support contact: cmp-support@mycmp.fr

Technology overview



AMF through CMC



CMC Microsystems announced that the organization will facilitate silicon photonics wafer runs through Advanced Micro Foundry (AMF) of Singapore with local European support from CMP.

CMP will be promoting AMF manufacturing services to its European client base in universities, research laboratories, and industrial companies. Read more

CMC offers this technology through a partnership with Advanced Micro Foundry (AMF)

Si-Photonics fabrication process AMF

TECHNOLOGY: AMF Si-Photonics	AMF Advanced Micro Foundry (AMF) Silicon Photonics Fabrication Process Silicon Photonic
Process characteristics	CMC Microsystems announced that the organization will facilitate silicon photonics wafer runs through AMF of Singapore with local European support from CMP. CMP will be promoting AMF manufacturing services to its European client base in universities, research laboratories, and industrial companies. CMC offers this technology through a partnership with Advanced Micro Foundry (AMF:http://www.advmf.com). Silicon-on-insulator, 220-nm top Si film, 2000-nm buried oxide (BOX) High resistivity handle wafer (>750 ohm-cm) 193-nm deep UV lithography for waveguides, enabling features down to approximately 140 nm Two partial etches and one full etch of the top silicon 6 implants for optical modulators (P++, P+, P, N++, N+, N) Germanium deposition and implanting for photodetectors Two metal levels, no planarization Front side oxide etch to selectively expose waveguides, e.g. for sensing applications Deep trench with etched facets for edge coupling Supports design and fabrication of a range of components and systems consisting of: - modulators - detectors - waveguides (strip or ridge) - gratings for fiber coupling - deep trench and nano-tapers for edge coupling - multiplexers (diffraction or arrayed waveguide) and filters (resonators, Bragg gratings) - ring and disk resonators
Application area	Interconnects, LIDAR, sensors and consumer optics
Design kits version	1.0
DK front-end/back-end tools	Mentor Graphics Pyxis Luceda-Tanner-AMF
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*

Contacts:

François BERTHOLLET
MPW Run Manager
Francois.Berthollet@mycmp.fr

Lyubomir KERACHEV
R&D Engineer / MPW Run Manager
Lyubomir.Kerachev@mycmp.fr

DK support contact: cmp-support@mycmp.fr

Micro Electro Mechanical Systems (MEMS) prototyping

In addition to ICs, OxRAM Non volatile Memory on 130nm processes, Si-Photonic technologies, CMP provides several types of MEMS technologies for prototyping and low volume production: Integrated bulk micromachining on CMOS technologies and specific surface micromachining technologies.

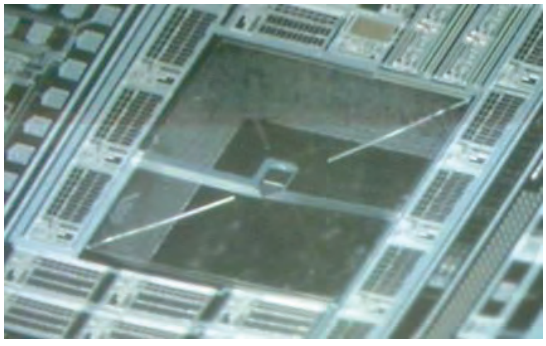
ams

0.35 µm Bulk Micromachining

This technology is based on standard CMOS or BiCMOS process allowing integration of MEMS sensor and front-end electronic on the same die for better signal to noise ratio. Suspended passive devices or structures can be made with this technology. Applications include thermal inertial sensors and infrared sensors.

TECHNOLOGY: Frontside Bulk Micromachining	ams MEMS Bulk Micromachining Frontside Bulk Micromachining CMOS FS Bulk Micromachining
Process characteristics	ams 0.35µ processes Process cross section Thick Metal module instead of Metal 4 module and with MIM capacitor module Poly layer(s): 2, high resistive poly Maximum die size: 2cm x 2cm DLP Usable cells: about 300 digital cells Available I/O: I/O cell library with digital pads is available 3.3V, 3V/5V, 5V with internal level shifters Temp. range: -40° C. / +125° C. Supply voltage: 5V or 3.3V Die size: Minimum charge of 3 mm²
Application area	MEMS, micromechanics, MOEMS
Design kits version	ams C35B4 4.10 ISR15
DK front-end/back-end tools	Cadence IC 6.1.6
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*

Front side bulk micromachining cross section

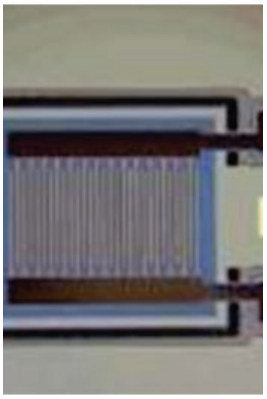


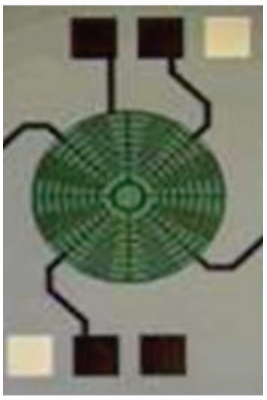
Bulk micromachining Backside, courtesy Tima

Contacts:

François BERTHOLLET
MPW Run Manager
Francois.Berthollet@mycmp.fr

Nicolas PARTENZA
MPW Run Manager
Nicolas.Partenza@mycmp.fr





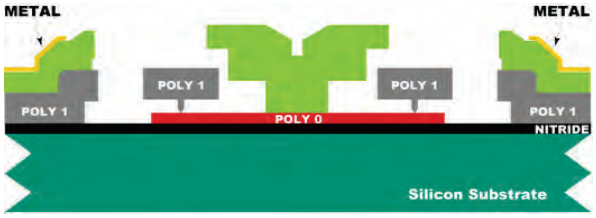
MEMSCAP

Created in 1997, MEMSCAP provides standard and custom innovative MEMS based solutions in market segments such as aerospace, medical/biomedical and telecommunications. Available through CMP since 1998, the Multi-User MEMS Processes (MUMPs) is a Multi Project Wafer program offering customers cost effective access to MEMS prototyping and low volume production through different processes: PolyMUMPs, SOIMUMPs and PiezoMUMPs.

PolyMUMPs

By removing the sacrificial layers, suspended structures can be made. Applications of PolyMUMPs include acoustic sensors (microphone), accelerometers, microfluidic devices and display technology.

TECHNOLOGY: PolyMUMPs	MEMSCAP MEMS Specific MEMS technologies PolyMUMPs MEMS MUMPS
Process characteristics	Fixed die size: 1cm x 1cm Polysilicon/gold Surface micromachining
Application area	MEMS, micromechanics, MOEMS
Design kits version	MEMS Pro v7.0
DK front-end/back-end tools	Cadence IC 6.1.5
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*

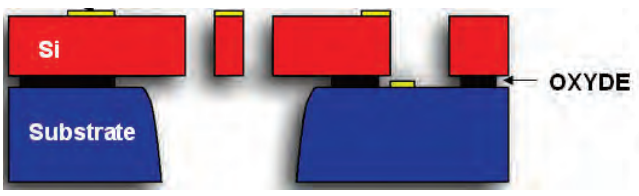


PolyMUMPs SEM cross section (Courtesy of MEMSCAP)

SOIMUMPs

Both sides of the SOI wafer can be patterned and etched up to the oxide layer through Deep Reactive Ion Etching (DRIE) allowing for through-hole structures and optical path. A shadow mask metal process is used to provide coarse metal structures such as bonding pads, electrical connections and optical mirror surfaces. A second metal layer can be used for bond pads and connectivity.
The 2µm feature size and structural layer thickness (10/15 µm) allow for gyroscope applications, whereas the through-hole capability and mirror surfaces can be used to design optical and display technology devices.

TECHNOLOGY: SOIMUMPs	MEMSCAP MEMS Specific MEMS technologies SOIMUMPs MEMS MUMPS
Process characteristics	Fixed die size: 0,9cm x 0,9cm SOIMUMPS + piezoelectric layer
Application area	MEMS, micromechanics, MOEMS
Design kits version	MEMS Pro v7.0
DK front-end/back-end tools	Cadence IC 6.1.5
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*



Cross section showing Reactive Ion Etching and Cross section of RIE etching (Courtesy of MEMSCAP)

Contacts:

François BERTHOLLET
MPW Run Manager
Francois.Berthollet@mycmp.fr

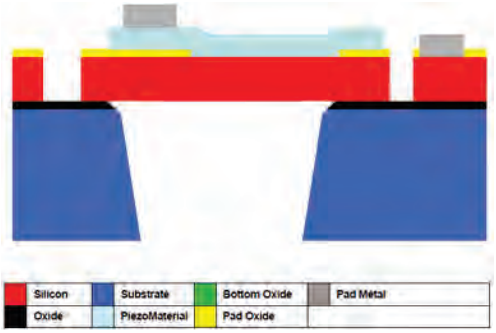
Nicolas PARTENZA
MPW Run Manager
Nicolas.Partenza@mycmp.fr

Technology overview

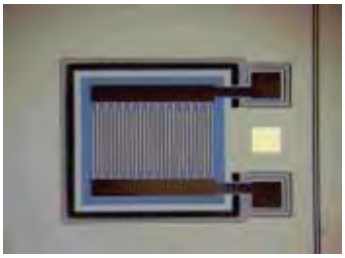
PiezoMUMPs

PiezoMUMPs is the most recent technology available through the MUMPs offer and was introduced in 2013. Based on a SOIMUMPs process (10 µm silicon thickness) it adds a 0.5 µm Aluminum Nitride piezoelectric layer. Active piezoelectric devices can be made with this process which permits development of energy harvesting applications, ultrasonic transducers, acoustic sensors or actuators.

TECHNOLOGY: PiezoMUMPs	MEMSCAP MEMS Specific MEMS technologies PiezoMUMPs MEMS PiezoMUMPS
Process characteristics	Fixed die size: 0,9cm x 0,9cm Deep Reactive Ion Etching on Silicon on Insulator
Application area	MEMS, micromechanics, MOEMS
Design kits version	1.1
DK front-end/back-end tools	Cadence IC 6.1.6
Price & Fabrication schedule	*Check mycmp.fr for new prices*
Packaging	*All packages provided by CMP*



PiezoMUMPs cross section and devices courtesy of MEMSCAP



PiezoMUMPs devices courtesy of MEMSCAP

Contacts:

François BERTHOLLET
MPW Run Manager
Francois.Berthollet@mycmp.fr

Nicolas PARTENZA
MPW Run Manager
Nicolas.Partenza@mycmp.fr

Standard packaging

Packaging is an important issue which can not be neglected for the complete success of a prototype production and implementation. The first step before starting a design is to select a package solution and a technology with respect to project constraints. Eventually, a standard package is needed and must be selected. In such a case, pad ring has to match with cavity of the selected package to optimize the whole interconnection. If the pad ring is not correct you will have to buy a dedicated package, this is time consuming and price can be significantly higher than price of silicon. General assembly rules and common errors are available on the Web site.

Wire-bond packaging process flow for MPW runs

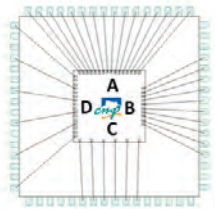
CMP offers a complete assembly service based on a wide range of ceramic and plastic packages for prototyping and low volume production.

Packaging guidelines

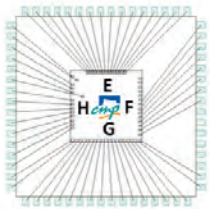
Prototypes packaging is a hard issue and yield can't be guaranteed. The pad ring of the circuit has to match the selected package to optimize the number of good samples. When you request bonding of additional circuits after runs you have to provide us with 5 additional dies for setup of the bonding machine. These dies can be damaged by setup.

At least the following simple rules have to be followed for prototypes in ceramic packages. They are not strong enough for low volume production:

- Bonding pads have to be connected to the side of the package that is facing.
- Use a homogenous spacing for pads with the first pad and the last pad near corners.
- Use the biggest width of bonding pad compatible with the number of pad in a side.
- All bonding pads should have the same size and are perfectly aligned along circuit edges.
- Bonding pad structure has to be strong enough to avoid stretch off when bonding wires.
- No bonding pad in corners.
- Avoid long wires. Check with us for wires longer than 4500µm.
- Angles of wires with the circuit edge have to be between 45° and 90°.
- A bonding wire can't cross another bonding wire (this generates a shortcut).



Correct



Incorrect

A: the best configurations.

B, C: good configurations when the number of pads is smaller.

D: dummy pads are correctly inserted.

E: pads are concentrated in the middle of the circuit's side.

F: dummy pads are concentrated on top (long wires and acute angles).

G: too many pads, pads in the corner, the 2 first pads and the 2 last pads are not connected to the package side that is facing.

H: pads are not aligned.

The diameter of wires used for a circuit depend on the side of the smallest pad of the circuit and on type of bonding (ball bonding or wedge bonding).

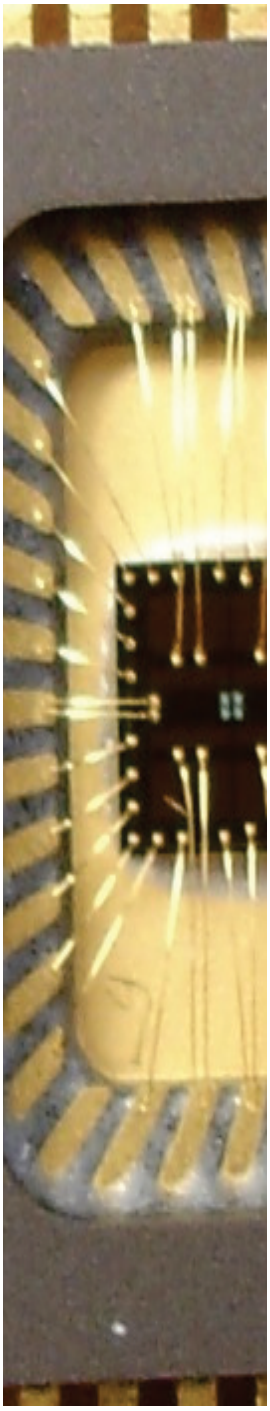
Some factors that are reducing yield:

- Long wire (shorts with neighbouring wires or with package cavity).
- Small pads (thin diameter for wires, risk to stretch wires off pads).
- Acute angles between wire and circuit edge (< 45°, shorts).
- Pads not perfectly aligned along the circuit edge (shorts).
- Pads incorrectly distributed in a side of the circuit (shorts).
- Bad bonding-pad structure (pad damaged by bonding).
- Bonding pads in corners (generation of crack on die).
- Big circuit ratio, length/width > 1.8 (long wires + acute angles).

Contact:

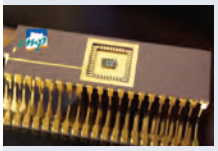
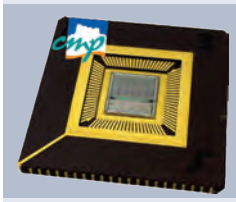
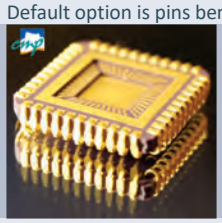
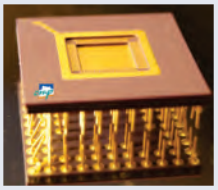
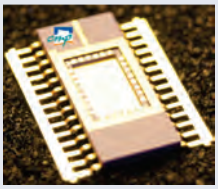
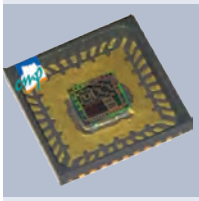
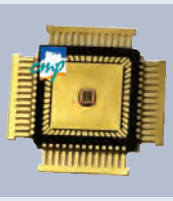
Jean-François PAILLOTIN
Lead Manager MPW Run/
STMicroelectronics
Jean-Francois.Paillotin@mycmp.fr

Technology overview



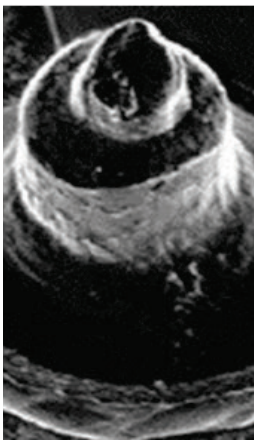
Available standard package types and associated services for prototyping & low volume production

CMP offers a wide variety of standard packages and assembly services for prototyping and low volume production. Before starting a design, an important step is to select a package and/or packaging technic. Die package compatibility optimization can significantly impact the overall system performances.
Prices & guidelines available on the Website.

Types & associated services & relevant features	
 Ceramic: Dual-in-line (DIL)	 Ceramic: CerQuad Flat Pack (CQFP) Up to 256 I/Os. *Available options for pins:* Z: gull wing J: Jleaded F: Flat Default option is pins bent in gull wing.
 Ceramic: C-Leaded Chip Carriers (CLCC)	 Ceramic/Plastic: J-Leaded Chip Carriers (JLCC)
 Ceramic: Pin Grid Arrays (PGA) Up to 352 pins	 Ceramic: Small Outline (SOIC)
 Plastic open cavity: Quad Flat Non Leaded (Open Cavity QFN) Thermal performance, low inductance, high frequency. Theses packages need thinned dies.	 Plastic open cavity: Thin Quad Flat Pad (TQFP) 25 samples minimum. Theses packages need thinned dies, lids must be sealed.
 Plastic Open Cavity Packages. Allow a smooth transfer between ceramic and plastic pakage (QFN, QFP, PLCC, PGA, BGA)	Optical resin, Chip On Board (COB), Thermal solutions, Metallic package & Hermetic package
Wafer level thinning ams 0.35µm (8”): standard thinning to 250µm ams 0.35µm (8”): thinning to 530µm on request only ST 130nm (8”): standard thinning to 375µm	Die level thinning Down to 150µm (absolute limit 100µm)
DRIE dicing Option of thinning to 50µm. Clean borders of the chips, a better precision than conventional dicing.	

Contact:

Jean-François PAILLOTIN
Lead Manager MPW Run/
STMicroelectronics
Jean-Francois.Paillotin@mycmp.fr



Courtesy HCM Systrel and LETI

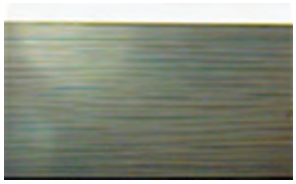
Contact:

Lyubomir KERACHEV
Technical Manager
Lyubomir.Kerachev@mycmp.fr

MEMS packaging

Several solutions are available for MEMS packaging: Optical resin/Transparent Lids/Chip On Board (COB)/Thermal solutions/Metallic package/Hermetic package.

Wafer and die thinning

Wafer level thinning	Die level thinning
ams 0.35µm (8"): standard thinning to 530µm ams 0.35µm (8"): thinning to 250 µm on request STMicroelectronics 130nm (8"): standard thinning to 375µm STMicroelectronics 65nm (12"): standard thinning to 250µm STMicroelectronics 28nm (12"): standard thinning to 250µm With this regular wafer level postprocess, die backside is smooth.	Down to 150 µm (absolute limit 100µm). Obtained with numerous saw kerfs over the entire backside of each IC.  *Die backside* With this solution, circuits' backside is a bit rough (10 to 25µm) with limited but possible issue for packaging.

Flip-Chip packaging

Compared to Wire-Bond packaging, Flip-Chip interconnects offer several advantages: decreased footprint, lower interconnect impedance allowing higher signal speed and better front side heat dissipation. CMP offers have been developed with the objectives of being technically reliable, being simple to support and to implement but also economically affordable.

When it comes down to choosing a Flip-Chip packaging method, there are several factors to be addressed:

- Fabrication of Interconnects realization on the silicon die.
- The substrate realization.
- The Flip-Chip assembly of the silicon die onto the substrate.

There are multiple ways to achieve each of the above steps, each of them having its own set of advantages and disadvantages. The eventual choice must take into account technical, budget and yield requirements. The different solutions offered by CMP will be described below. For more information on CMP flip-chip offers, please contact the CMP engineer in charge of FC packaging at ajith-sivadasan.moreau@mycmp.fr. You must anticipate your choice of packaging in the very early stage of your project and notify it within your reservation form.

Fabrication of interconnects realization on the silicon die

Three types of Flip-Chip interconnects are accessible through CMP: µ-Bumps (or copper pillars), Solder balls and Gold stud-Bumps. The following section will discuss the technical differences as well as their accessibility through CMP.

STMicroelectronics Copper-pillar Interconnections

Copper pillars are manufactured at wafer-level by STMicroelectronics. This interconnection is composed of an Under Bump Mettalization (UBM), upon which a pillar of copper is grown, a capping of Sn/Ag allows the die to be assembled on a substrate by reflow process. The dimensions of this copper pillar are approximately 62 µm in diameter for 65 µm in height, thus allowing a fine pitch (down to 90 µm).

Accessibility conditions:

- Copper pillar option is available on CMOS28FDSOI and BiCMOS055 MPW and dedicated runs as options. For compatibility with other technologies, please refer to µ-bumps interconnections section below.
- FC44S pad class must be used in the design to be compatible with this option.
- Check for prices: contact CMP.

Courtesy of LETI

Contact:

Lyubomir KERACHEV
Technical Manager
Lyubomir.Kerachev@mycmp.fr

Copper-pillar interconnections at die-level

CMP is now able to offer manufacturing of copper pillars at die-level. The dimensions of these copper pillars are approximately 60µm in diameter for 45µm height plus 20µm solder height allowing fine pitch down to 90µm. A SnAg with 1.80% Ag solder cap is deposited on the copper pillars to ensure the electrical contact.

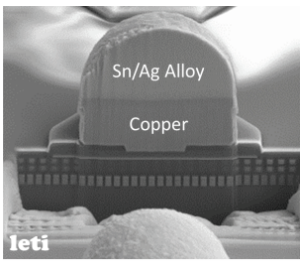
Accessibility conditions:

This die-level copper pillar option is available on any silicon process. The price is design dependent and is a fraction of current costs.

Micro-Bumps interconnections

Similar to the copper pillars in terms of technology, micro-bumps are manufactured at wafer-level as a post-process within CEA LETI cleanroom. This interconnection is composed of a pillar of copper upon which a Sn/Ag alloy is deposited to ensure electrical contact. This technology offer from CEA LETI allows for a very fine pitch (down to 50 µm) and offers improved electro migration performances compared to solder bumps. The process-steps are described below :

- Seed Layer (or UBM) deposition
- Copper electro-deposition (requires masking)
- Sn/Ag alloy deposition
- Seed layer etching and reflow



Accessibility conditions:

- As an MPW OPEN3D µ-bumps post-process: Diameter and height are set to 25µm/20µm with a 50 µm minimum pitch. OPEN 3D MPW post-process options are available on the last CMP run of the year on selected technologies nodes and are subject to a minimum participation. Check for new prices: mycmp.fr
- As a dedicated OPEN3D µ-bumps post-process: Diameter/height pair is not imposed and can be chosen within process window. OPEN 3D dedicated µ-bumps post-process option is available on any CMP runs (upon feasibility study). Check for new prices: mycmp.fr

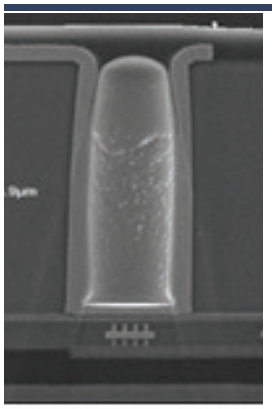
OPEN 3D post-process must be anticipated at an early stage of the project as they require an additional NDA, the distribution of a specific DRM and an add-on to the Design-Kit (please refer to the advanced packaging section for more information). This must be indicated in the reservation form.

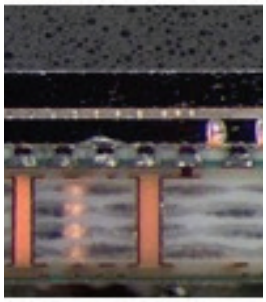
Solder Bumps interconnection

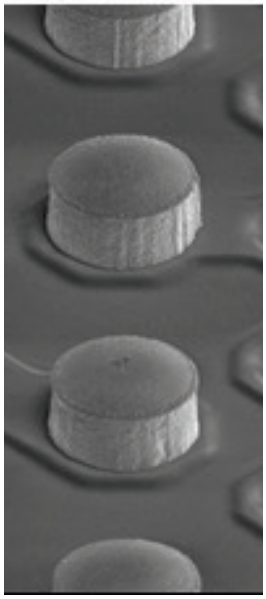
Solder bumping consists of manufacturing metal spheres acting as interconnections for flip-chip. Those spheres are composed of a Sn/Ag/Cu alloy (SAC). Prior to the metal sphere deposition, the deposition of an Under Bump Metalization (UBM) layer is required. Several solutions for solder bumping are available at CMP and they are discussed below.

ams solder bumping finishing

This option, available only on ams runs, is performed at wafer-level within ams cleanroom after CMOS process. It allows the deposition of an array of solder balls at wafer-level, with an I/O pitch compatible with traditional printed circuit board (PCB) assembly processes. For mechanical reasons solder balls are usually evenly distributed over the whole chip surface and electrically connected to the IC's CMOS pads by means of a redistribution layer (RDL) included in the option.







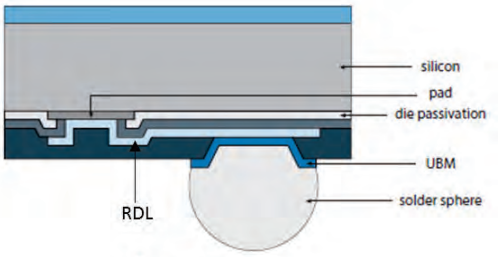
Courtesy of LETI

Contact:

Lyubomir KERACHEV
Technical Manager
Lyubomir.Kerachev@mycmp.fr

Image courtesy of ams

Top View



Cross section

Accessibility conditions:
ams Wafer-level bumping option with RDL is supported within ams design kit through an add-on and upon request.
It is available on any 0.35 ams MPW runs. Check for prices: mycmp.fr

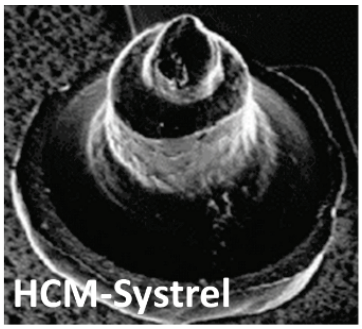
Solder bumping post-process

This post-process is not offered by the IC foundry but by an external subcontractor. This is a two-steps process: first, an electro less UBM (Ni/Au) is deposited on the pads of the die, then solder balls are individually placed over the pads. The minimum pitch is 150 µm.

Accessibility and conditions:
The price of this option depends on the design, you must request a quotation at the early stage of your project.

Gold stud bump interconnections

Stud bump bonding interconnections are manufactured at die-level with a Wire-Bonding equipment. The ball is bonded to the die pad with a gold wire which is then cut right above the ball. The resulting interconnection allows flip-chip assembly of the die onto a substrate by thermocompression or thermosonic process. Stud bumping does not require UBM or RDL underneath the balls.



Accessibility conditions:
Gold stud bumping option is available on any MPW run processed through CMP. The price of this option depends on the design, and the users are advised to request a quotation at the early stage of your project.

Substrate realization

Depending on the pitch of the flip-chip interconnections, the die can either be directly assembled on a PCB board or may require an intermediate substrate. Two types of substrate materials are available through CMP: plastic and ceramic.

Accessibility conditions:
Custom designed plastic and ceramic substrate: if your project requires a custom designed substrate, CMP can work with its subcontractors to deliver it. CMP will then help you through the different steps of the project by:

- Verifying Die/Substrate compatibility before fabrication
- Ensuring the technical information exchange with our subcontractor on your behalf
- Optimizing turnover by coordinating the different links of the packaging chain (die and substrate fabrication, flip-chip interconnection realization and assembly on substrate)

The price of this option depends on the substrate specifications, and users are advised to request a quotation at the early stage of your project. This option is available on any CMP MPW runs.

Technology overview

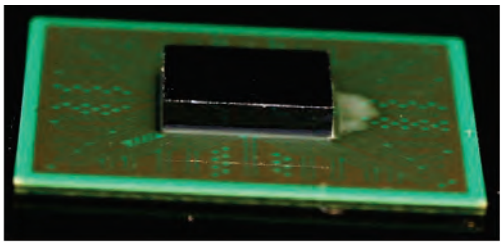
Flip-Chip assembly

The third and last point to address is the assembly of the chip onto the substrate or PCB (as “chip on board”). The choice of subcontractors as well as the choice of assembly technique (mass reflow, thermocompression, thermosonic…) depends on the type of chip, interconnect and substrate used in the project, directly impacting the price of the service. Request for a quote at the early stage of your project is advised.

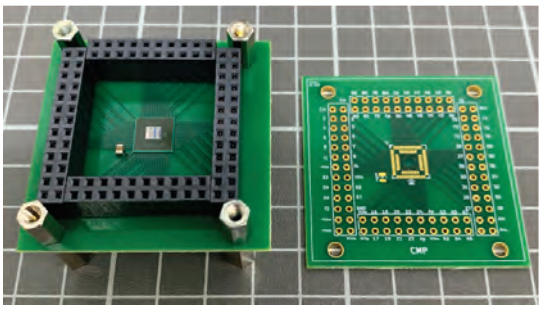
CMP realized evaluation of a full flip-chip assembly process using bare dies and LGA substrates. The dies and the substrates were co-designed considering the design rules of both ASIC and substrate manufacturers, and the post-process technological constraints.
Several manual post-process steps were done in order to realize the flip-chip assembly:

- die level UBM electroless Ni/Au plating ;
- die level solder bumping using SAC305 solder bumps with 70um diameter;
- LGA substrate manufacturing;
- Flip-chip of the bare dies on the LGA substrates;
- Underfill deposition;
- Mounting of the realized assemblies on standard test PCBs.

The following image is a photo of the realized prototype. The result of this manual non-standard process is 75% yield including the material used for the setup.



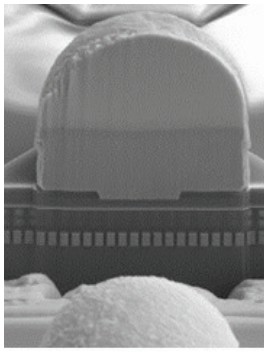
1. Flip-chipped die on LGA substrate

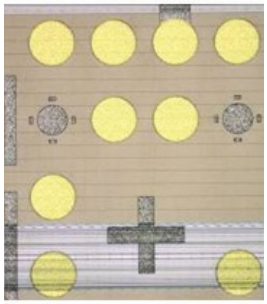


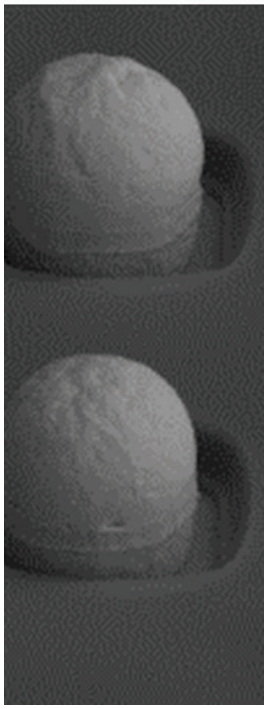
2. LGA substrate mounted on a PCB test board

Contact:

Lyubomir KERACHEV
Technical Manager
Lyubomir.Kerachev@mycmp.fr







Courtesy of LETI

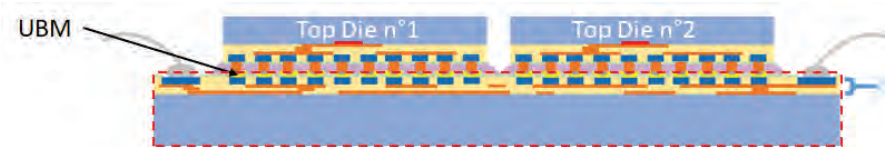
Contact:

Lyubomir KERACHEV
Technical Manager
Lyubomir.Kerachev@mycmp.fr

Advanced packaging

Silicon interposer

CMP offers a 2.5D integration solution through specific MPW runs for silicon interposer production, allowing side by side integration of heterogeneous dies with higher interconnection density than organic substrates, thus contributing to package footprint reduction, increased inter-die bandwidth and decreased power consumption.
This interposer offer is based on 0.35µm metal stack (including up to 4 metal levels for routing), upon which a post-process is performed in order to produce a front-side Under Bump Metalization (or UBM) consisting of Ni/Pd/Au stack.
The resulting interposer is ready to support flip-chip dies and is compatible with CMP OPEN 3D micro-bumps post-process offer (with a 50µm min pitch). The interposer includes Wire-bonding pads to allow its connection to a PCB (as chip on board) or a compatible package.



Silicon interposer

Two options are available for Silicon interposer prototyping:

- **Passive interposer: o**nly the back end is processed, for high density routing applications and passive component integration.
- **Active interposer: a**ctive layers are available for CMOS integration, allowing the implementation of a wider range of functions within the interposer.

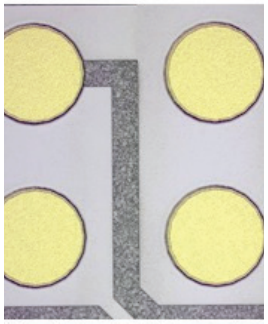
Access to this silicon interposer offer is initiated through a formal DK request as well as an approval from the CMP administration and associated partners through our web interface. Interposer run offer is available at any time of the year. Note that this interposer is compatible with OPEN 3D TSV backside post-process.

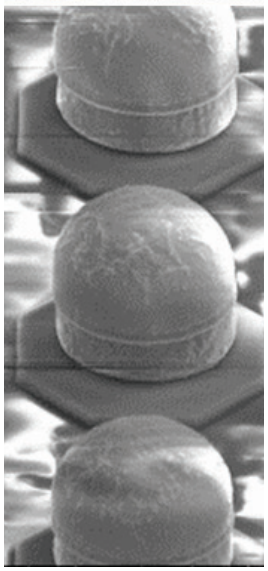
TECHNOLOGY	**4M interposer**
Design kits	Distributed by CMP on request
DRM	Provided by CMP on request
Fabrication schedule	Upon request
Price & Fabrication schedule	Check mycmp.fr for new prices
Quantity	30 chips guaranteed. We can deliver more on request
Typical Turnaround time	23 weeks

OPEN 3D post-process for 3D integration

CMP, in partnership with CEA-LETI, offers a set of post-processes allowing various types of 3D assemblies. Those post-processes are operated at wafer-level and are carried out after standard MPW runs on a selected subset of technologies. The goal is to integrate 3D interconnections to chips processed through CMP, in order to enable flip-chip on organic or ceramic substrates as well as Die-to-Die or Die-to-Interposer assemblies.

Technology overview





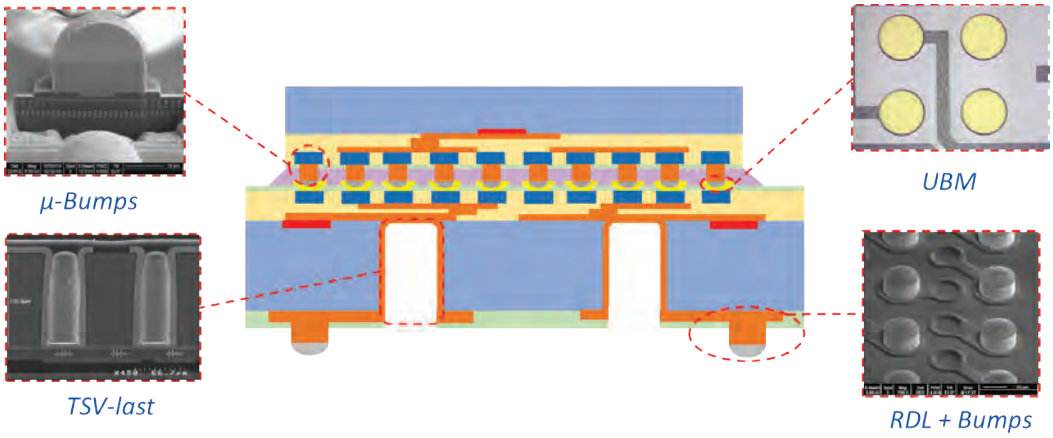
Courtesy of LETI

Contact:

Lyubomir KERACHEV
Technical Manager
Lyubomir.Kerachev@mycmp.fr

Two types of post-processes are made available, including different options:

- **Front-side:** 3D interconnections (µ-Bumps or UBM).
- **Back-side:** Wafer thinning, TSV (via-last) and RDL, 3D interconnections (Bumps).



3D integration of two Si-dies

Post-processes made available after MPW runs gives CMP users the opportunity to have access to advanced packaging techniques on compatible nodes. OPEN 3D post processing is available upon request, please contact ajith-sivadasan.moreau@mycmp.fr for more information on packaging solutions for your project. For further specific information on OPEN 3D modules (size, pitch, thickness…), please refer to the table below as well as additional information on CMP Website.

Technical information

µBumps (Cu-pillar)	Cu/SnAg ; ø25 µm ; 50 µm min pitch ; ~20 µm thickness
UBM	TiNiAu ; 25 µm min width; 50 µm min pitch ; 1 µm thickness
TSV-LAST	Ø60 µm x 120 µm depth ; 120 µm min pitch
Backside RDL	Cu ; 20 µm min width ; 40 µm min pitch ; 4-8 µm Thickness

Accessibility conditions:

- As a MPW OPEN3D Front-side post process (µ-Bumps or UBM)
- As a MPW OPEN3D Back-side post process (TSV, RDL and Bumps)
- As a MPW OPEN3D Back-side + Front-side post process (µ-Bumps or UBM + TSV, RDL and Bumps)

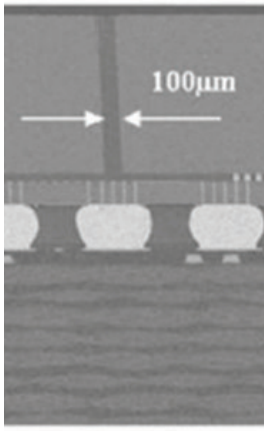
MPW OPEN 3D post processes are available for projects and wafers processed through CMP on the last CMP MPW run of the year for the following technologies: STMicrolectronics : CMOS28FDSOI (frontside only), BiCMOS055, CMOS065, BiCMOS9MW, LETI : Silicon Photonic and **ams** : C35B4M3. Those runs are subject to a certain minimum number of participants sharing the MPW.

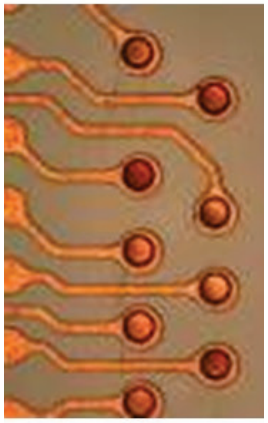
MPW OPEN 3D post-processes must be anticipated at an early stage as they require an additional NDA, the distribution of a specific DRM and an add-on to the Design-Kit. Additionaly, this must be indicated it in the reservation form.

- As a dedicated OPEN3D post-process

Dedicated OPEN3D post processes can be made available on any CMP MPW Run at any time of the year after a feasibility study. In this case, restrictions to specific geometrical parameters of the design structure are not imposed and can be chosen within a process window. Please contact CMP for more information/quotation.

Check for new prices: mycmp.fr





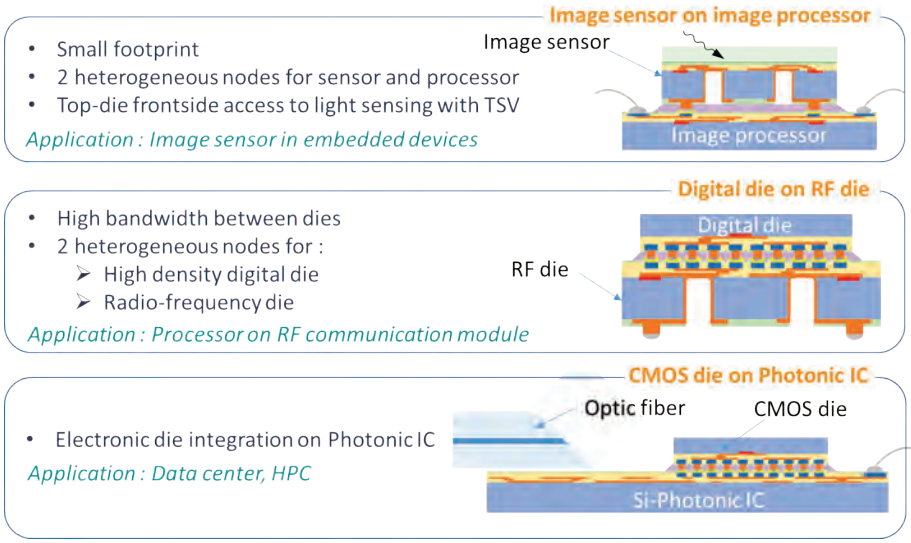
Courtesy of LETI

Contact:

Lyubomir KERACHEV
Technical Manager
Lyubomir.Kerachev@mycmp.fr

OPEN3D post-process application examples

Leti OPEN 3D post-processes allows the manufacturing of 3D modules, where chips based on different technolgy nodes can be stacked one above the other. Thanks to this, numerous multi-die architectures can be realized. The next section introduces several such 3D structures with their corresponding applications.



Application examples

3D post-processed chips design, verification and manufacturing flow

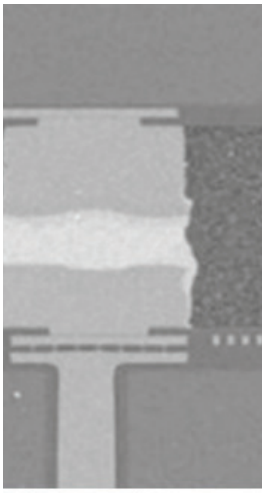
Post-processed wafers, from which are extracted ICs, results from the combination of two technologies which requires special considerations during design, verification and fabrication. The goal of this section is to describe how ICs, dedicated to advanced packaging, are processed each step of the way.

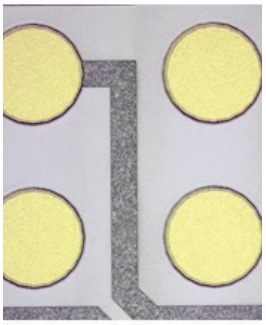
3D post process design tools

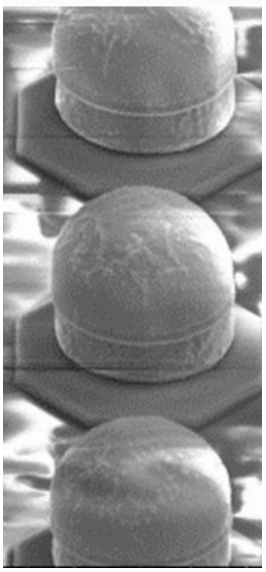
In order to facilitate design of ICs undergoing a 3D post process, CMP and LETI have co-developed a 3D Kit allowing the implementation of additional layers required for 3D modules manufacturing. This Kit works as an add-on applied to the original foundry DK and it contains:

- Open 3D post-process technology integration to Cadence, alongside the original technology.
- A library of several ready-to-use 3D modules (Bumps, µ-bumps, TSV…)
- A calibre die-level DRC Deck to check the design conformity to Open 3D Design Rules Manual.

This 3D kit alongwith the Open 3D DRM, allows designers to easily integrate 3D modules to their designs. In addition to the 3D Kit, a calibre assembly-level DRC Deck (3DSTACK) checks the additional rules specific to silicon-on-silicon assemblies (such as the verification of electrical connections between dies). The development of a custom assembly-level DRC is required for every 3D project, and is a part of CMP service to help the designer on their 3D projects. Please note that this Assembly-level DRC is not distributed to CMP users, but they have access to DRC results and comments.







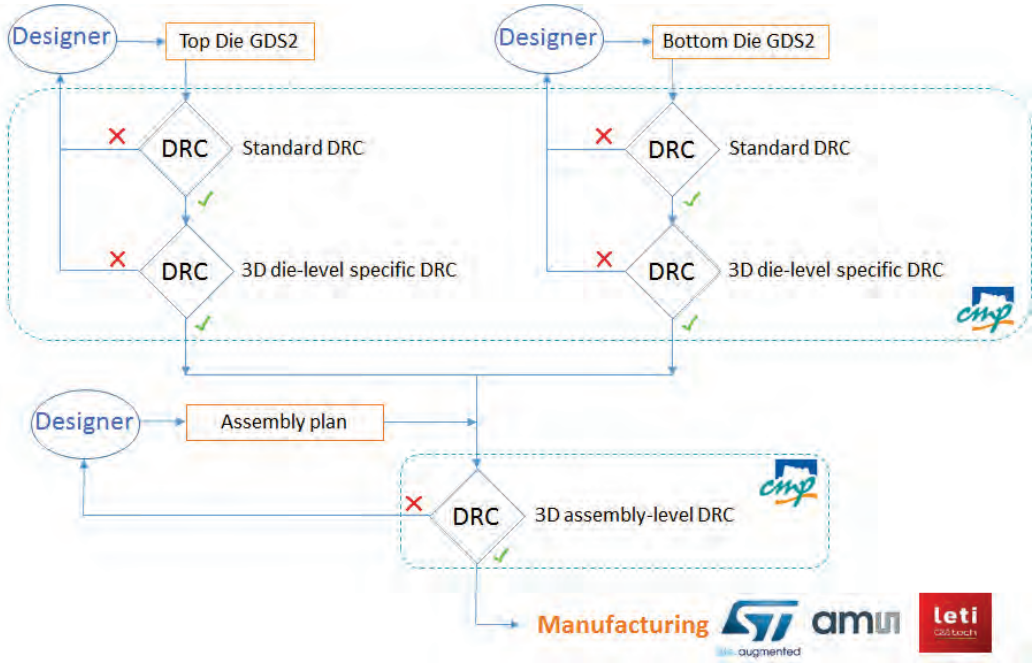
Courtesy of LETI

CMP contact:

Lyubomir KERACHEV
Technical Manager
Lyubomir.Kerachev@mycmp.fr

CMP verification flow

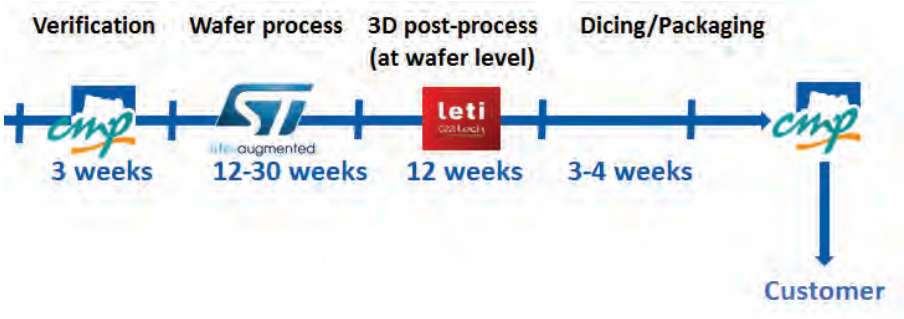
Upon receipt of the GDSII from the deisgner, that contains information of both technologies, verification process is initiated. CMP treatment of 3D circuits is slightly different from that of classical ones in a way that both processes' compliance is verified. Furthermore, for silicon-on-silicon assembly only, an additional verification step is carried out to check the whole assembly at once. The following graph illustrates the verification flow of a die-to-die assembly.



Verification flow

Manufacturing flow example

3D post-processed dies involve two different foundries. The following graph illustrates this process for bumps manufacturing on an ST processed wafer. The wafers are first processed on a 65 nm node at STMicroelectronics. Once the process is complete, wafers are sent to CEA-LETI cleanroom where they will undergo bumps fabrication process. Wafers are then diced, sent back to CMP before they are shipped to the customer.



Bumps manufacturing process

From Layout to Chips
mycmp.fr

MPW run schedule

Multiproject wafer (MPW) fabrication runs scheduled:

STMicroelectronics	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
IC 28nm CMOS28FDSOI		10							14			
IC 55nm BiCMOS055		17	26				27					
IC 65nm CMOS065		4							30			
IC 130nm BiCMOS9MW			2			2					2	
IC 0.16µm BCD8sP			13							2		
IC 0.16µm BCD8s-SOI		21								2		
ams	**Jan**	**Feb**	**Mar**	**Apr**	**May**	**Jun**	**Jul**	**Aug**	**Sep**	**Oct**	**Nov**	**Dec**
IC 0.35µm BARC C35B4OA	10*				22*				19*			
IC 0.35µm C35B4C3	10				22				19			
IC 0.35µm ARC C35B4O1 IC 0.35µm BARC C35B4OA	10*				22*				19*			
IC 0.35µm H35B4D3					11							
IC 0.35µm S35D4M5						15						
ON Semiconductor	**Jan**	**Feb**	**Mar**	**Apr**	**May**	**Jun**	**Jul**	**Aug**	**Sep**	**Oct**	**Nov**	**Dec**
IC 0.18µm CMOS ONC18MS	10			14		15		17		22		14
IC 0.18µm CMOS HV ONC18I4T	10			14		15		17		22		14
IC 0.35µm CMOS ONC35U		3		21			8		21			8
IC 0.35µm CMOS HV ONC35I3T25U		3		21			8		21			8
IC 0.35µm CMOS HV ONC35I3T50U			9			2			8			8
em microelectronic	**Jan**	**Feb**	**Mar**	**Apr**	**May**	**Jun**	**Jul**	**Aug**	**Sep**	**Oct**	**Nov**	**Dec**
IC 0.18µm CMOS EMALPC18 logic				24			15			30		
IRT Nanoelec/LETI-CEA	**Jan**	**Feb**	**Mar**	**Apr**	**May**	**Jun**	**Jul**	**Aug**	**Sep**	**Oct**	**Nov**	**Dec**
Silicon Photonic ICs Si310-PHMP2M			20							16		
AMF	**Jan**	**Feb**	**Mar**	**Apr**	**May**	**Jun**	**Jul**	**Aug**	**Sep**	**Oct**	**Nov**	**Dec**
Si-Photonics fabrication process AMF							3				4	
MEMSCAP	**Jan**	**Feb**	**Mar**	**Apr**	**May**	**Jun**	**Jul**	**Aug**	**Sep**	**Oct**	**Nov**	**Dec**
MEMS Specific MEMS technologies PolyMUMPs	14			21				4			17	
MEMS Specific MEMS technologies SOIMUMPs			3			2			1			8
MEMS Specific MEMS technologies PiezoMUMPs	28				19				8			

Notes:

- *On request. Reservation should be done 8 weeks before the deadline
- All MPW scheduled runs are subject to modification.
- *MPW OPEN 3D post processes are available for projects and wafers processed through CMP on the last CMP MPW run of the year for the following technologies:* ***STMicrolectronics*** *: CMOS28FDSOI (frontside only), BiCMOS055, CMOS065, BiCMOS9MW,* ***LETI*** *: Silicon Photonic and* ***ams*** *: C35B4M3. Those runs are subject to a certain minimum number of participants sharing the MPW.*

*On request. Reservation should be done 8 weeks before the deadline

From Layout to Chips
mycmp.fr

Contact information

Staff members and their current responsibilities.

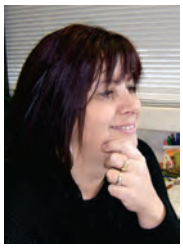
Contact details of staff members:

Isabelle AMIELH
+33 4 76 57 46 17
Chief Administrative Officer
Isabelle.Amielh@mycmp.fr

Chantal BÉNIS-MOREL
+33 4 76 57 46 22
Communication Officer
Chantal.Benis@mycmp.fr

François BERTHOLLET
+33 4 76 57 46 21
MPW Run Manager
Francois.Berthollet@mycmp.fr

Alejandro CHAGOYA
+33 4 56 52 89 23
Senior IT Manager & Design-Kit Support
Alexandre.Chagoya@mycmp.fr



Patricia CHASSAT
+33 4 76 57 47 47
Secretariat & Shipments
Patricia.Chassat@mycmp.fr

Sylvaine EYRAUD
+33 4 76 57 46 79
Design-Kit Admin. Manager
Sylvaine.Eyraud@mycmp.fr

Lyubomir KERACHEV
+33 4 76 57 48 34
Technical Manager
Lyubomir.Kerachev@mycmp.fr

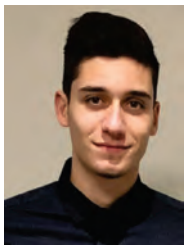
Valentin LANCELOT
+33 4 76 57 49 87
Webmaster
Valentin.Lancelot@mycmp.fr

Aurélien NICOLET
+33 4 76 57 46 05
Project Manager
Aurelien.Nicolet@mycmp.fr

Contact information

Jean-François PAILLOTIN
+33 4 76 57 47 97
MPW Run Lead Manager
Jean-Francois.Paillotin@mycmp.fr

Joëlle PARRAU
+33 4 76 57 46 14
Accounting and Human Resources
Joelle.Parrau@mycmp.fr



Nicolas PARTENZA
+33 4 76 52 89 19
MPW Run Manager
Nicolas.Partenza@mycmp.fr

Jérémy PERRET
+33 4 76 57 47 48
Project Manager
Jeremy.Perret@mycmp.fr

Christelle RABACHE
+33 4 76 57 46 19
Technical Manager
Christelle.Rabache@mycmp.fr

Kholdoun TORKI
+33 4 76 57 47 63
Director
Kholdoun.Torki@mycmp.fr

Romain VERLY
+33 4 76 57 48 65
MPW Run Manager
Romain.Verly@mycmp.fr

Yann YEBE
+33 4 76 57 46 47
Design-Kit Support Engineer
yann.yebe@mycmp.fr

From Layout to Chips
mycmp.fr